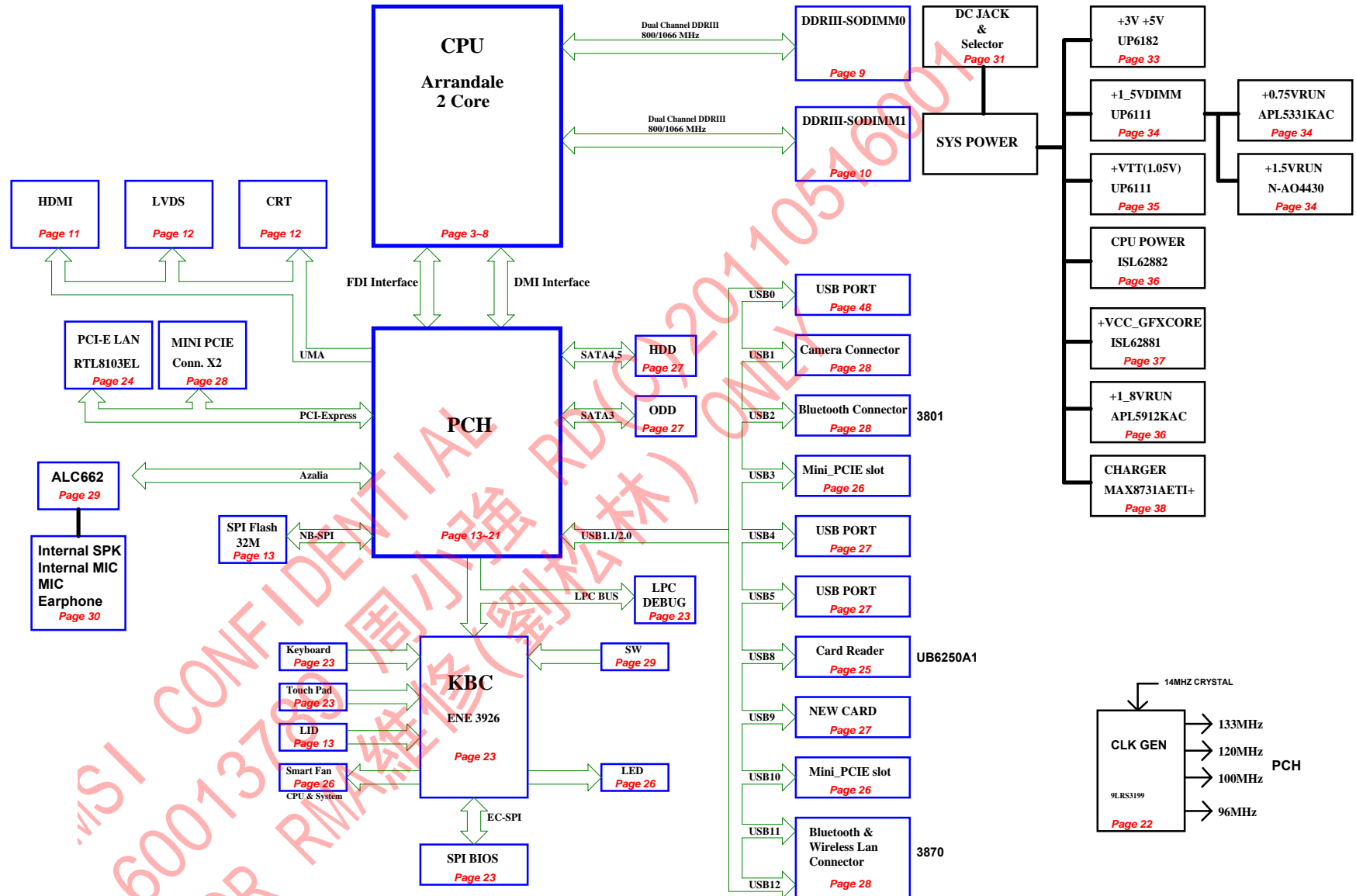


Calpella Platform

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41_EMI
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

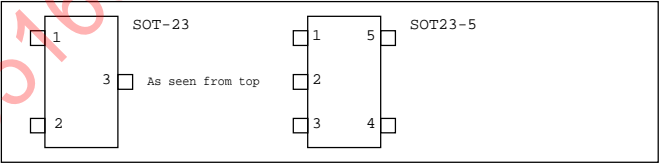
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	LAN
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	DDRIII core
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	
+1_5VRUN	1.5V	S0	PCH DDRIII command & control pull up. CPU core rail Graphics core rail (Dual Core only)
VTT	1.05V	S0	
+0_75VRUN	0.75V	S0	
+VCC_CORE	1.05V~1.1V	S0	
+VCC_GFXCORE	1.1V	S0	

Net Naming Conventions

Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



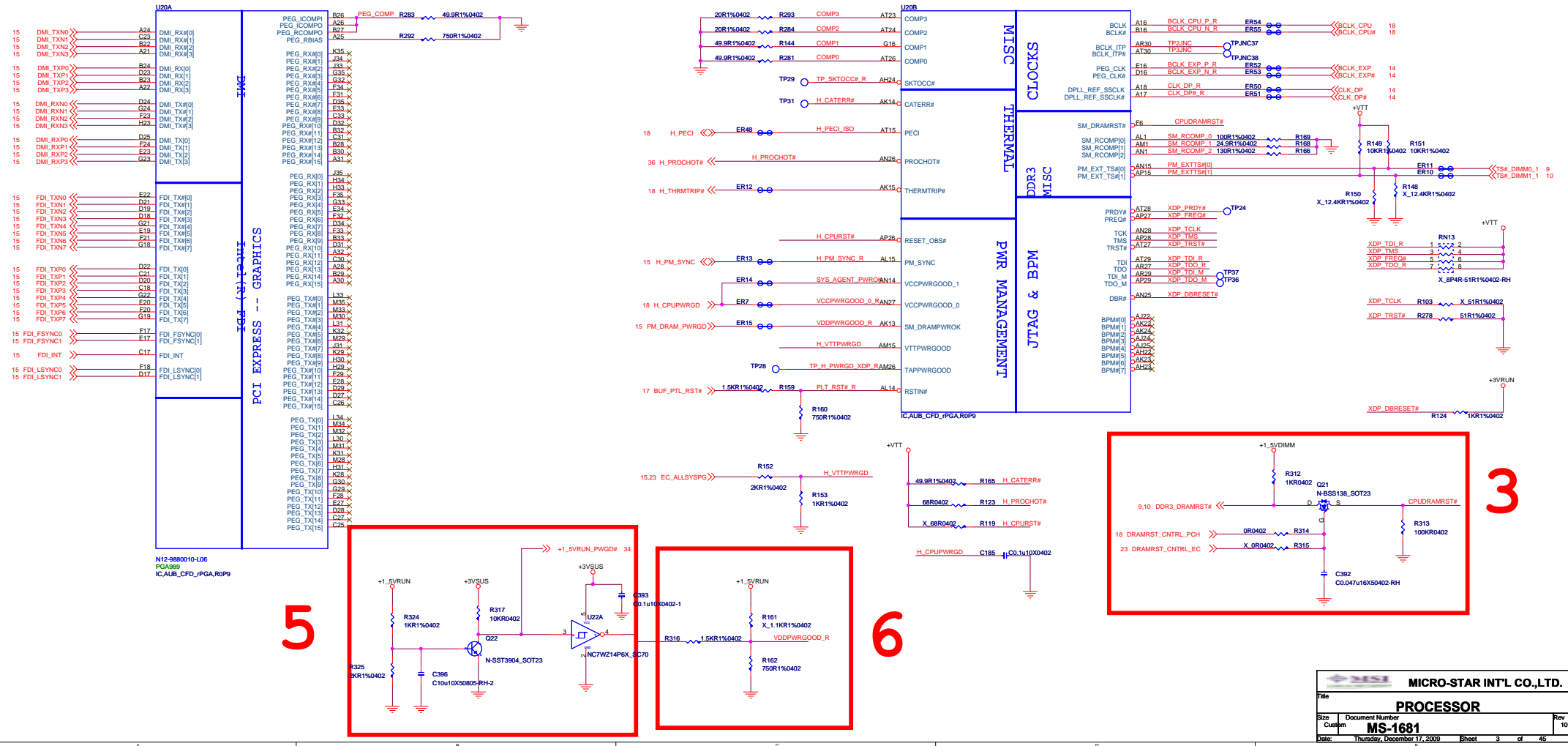
AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

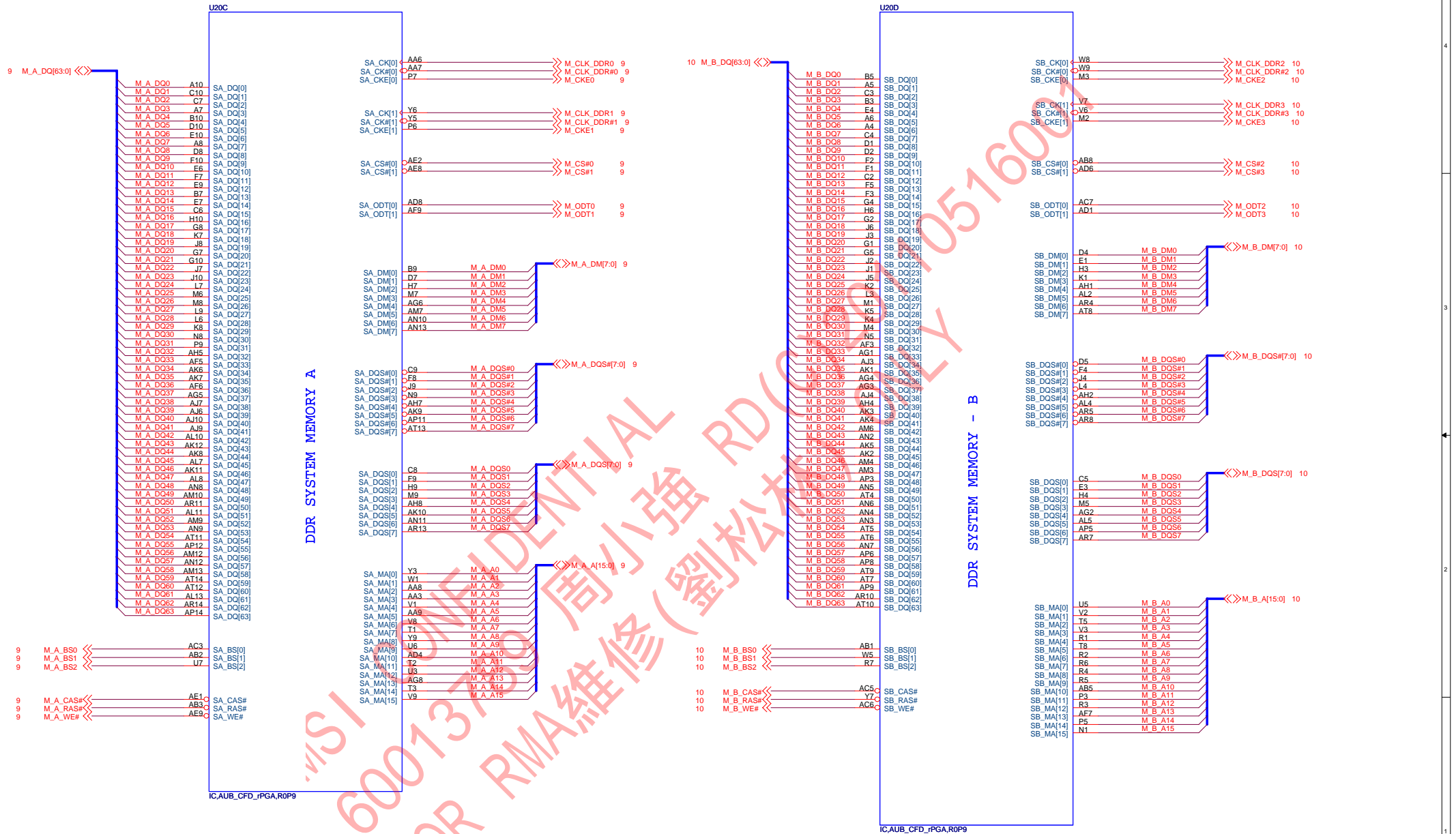
Battery Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

ARRANDALE PROCESSOR (CLK,MISC,JTAG)



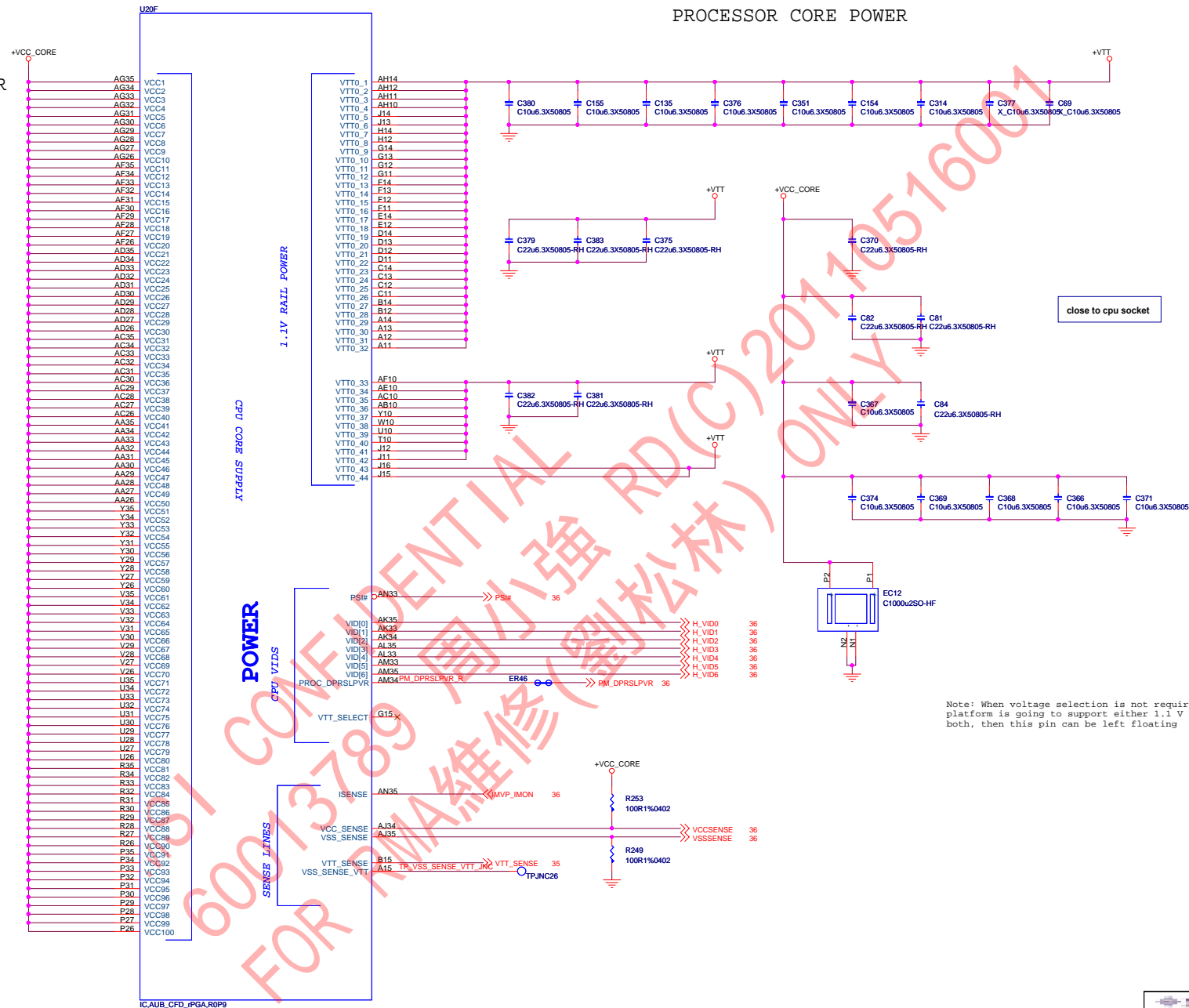
ARRANDALE PROCESSOR (DDR3)



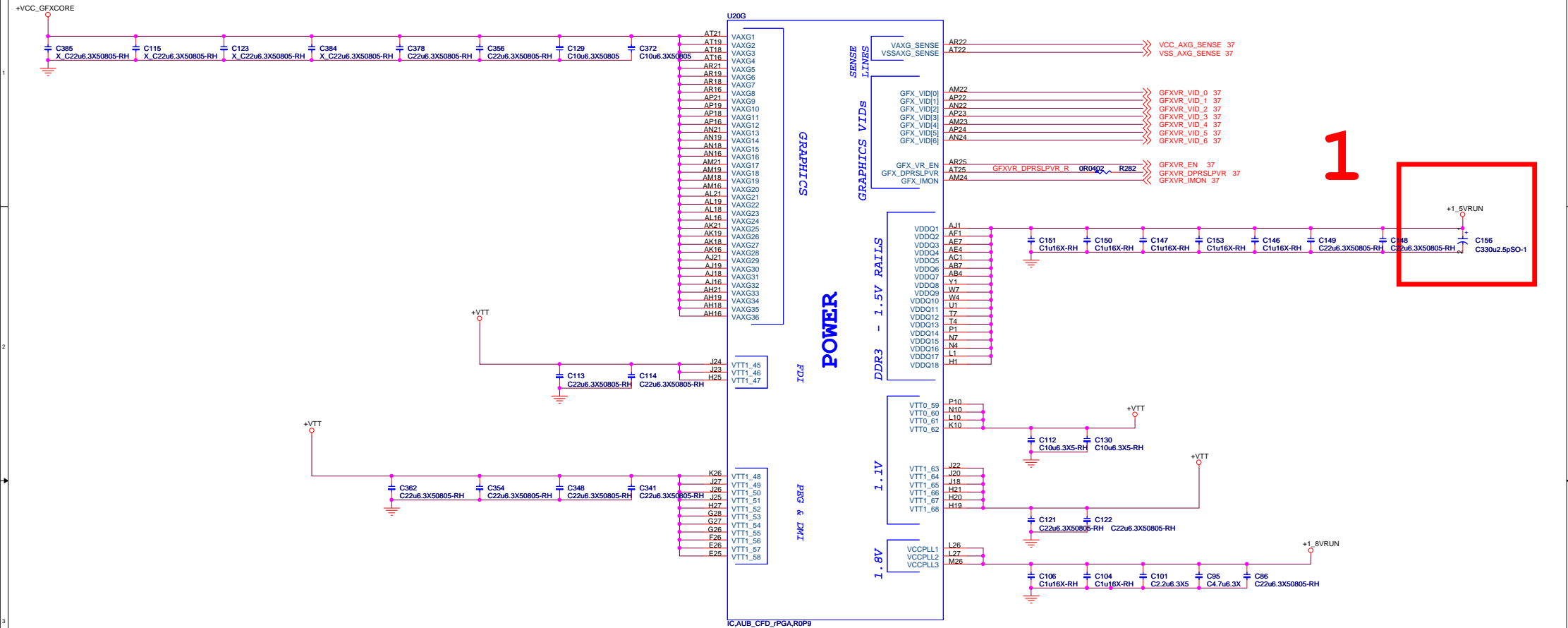
ARRANDALE PROCESSOR (POWER)

PROCESSOR CORE POWER

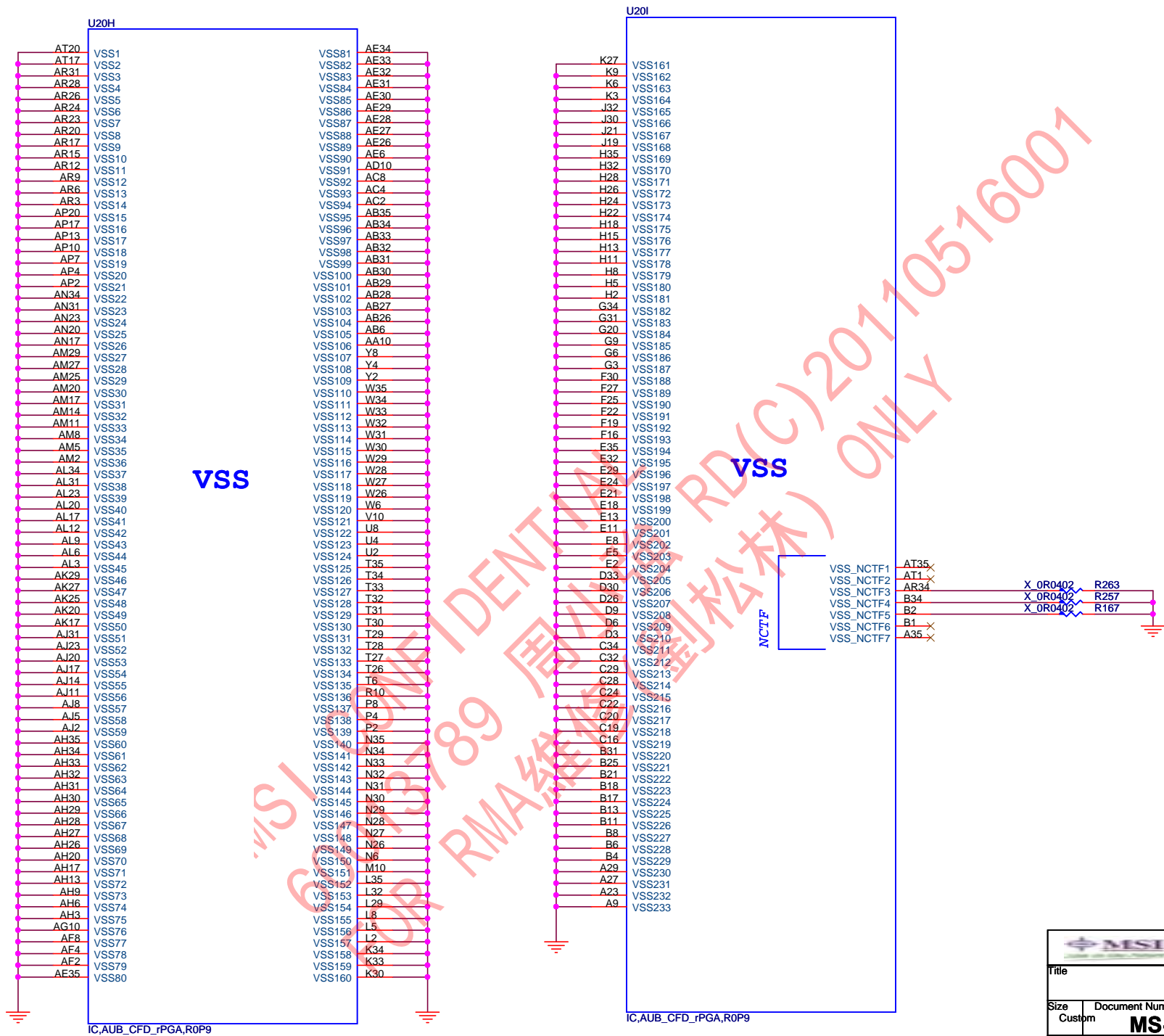
PROCESSOR CORE POWER



ARRANDALE PROCESSOR (GRAPHICS POWER)



ARRANDALE PROCESSOR (GND)



ARRANDALE PROCESSOR (RESERVED)

U20E

AP25
AL25
AL24
AL22
AJ33
AG9
M27
L28
J17
H17
G25
G17
E31
E30

RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14

TP25
TP17
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B19
A19
A20
B20

U9
T9
AC9
AB9

C1
A3

J29
J28

A34
A33

C35
B35

IC_AUB_CFD_rPGA,R0P9

RESERVED

RSVD32
RSVD33

RSVD34
RSVD35

RSVD36
RSVD_NCTF_37

RSVD38
RSVD39

RSVD_NCTF_40
RSVD_NCTF_41

RSVD_NCTF_42
RSVD_NCTF_43

RSVD45
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RSVD51
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RSVD53
RSVD54

RSVD_NCTF_55
RSVD_NCTF_56

RSVD_NCTF_57
RSVD58

RSVD_TP_59
RSVD_TP_60

KEY
RSVD62

RSVD63
RSVD64

RSVD65

RSVD_TP_66
RSVD_TP_67

RSVD_TP_68
RSVD_TP_69

RSVD_TP_70
RSVD_TP_71

RSVD_TP_72
RSVD_TP_73

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RSVD_TP_75

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RSVD_TP_109

RSVD_TP_110
RSVD_TP_111

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AJ12

AH25
AK26

AL26
AR2

AJ26
AJ27

AP1
AT2

AT3
AR1

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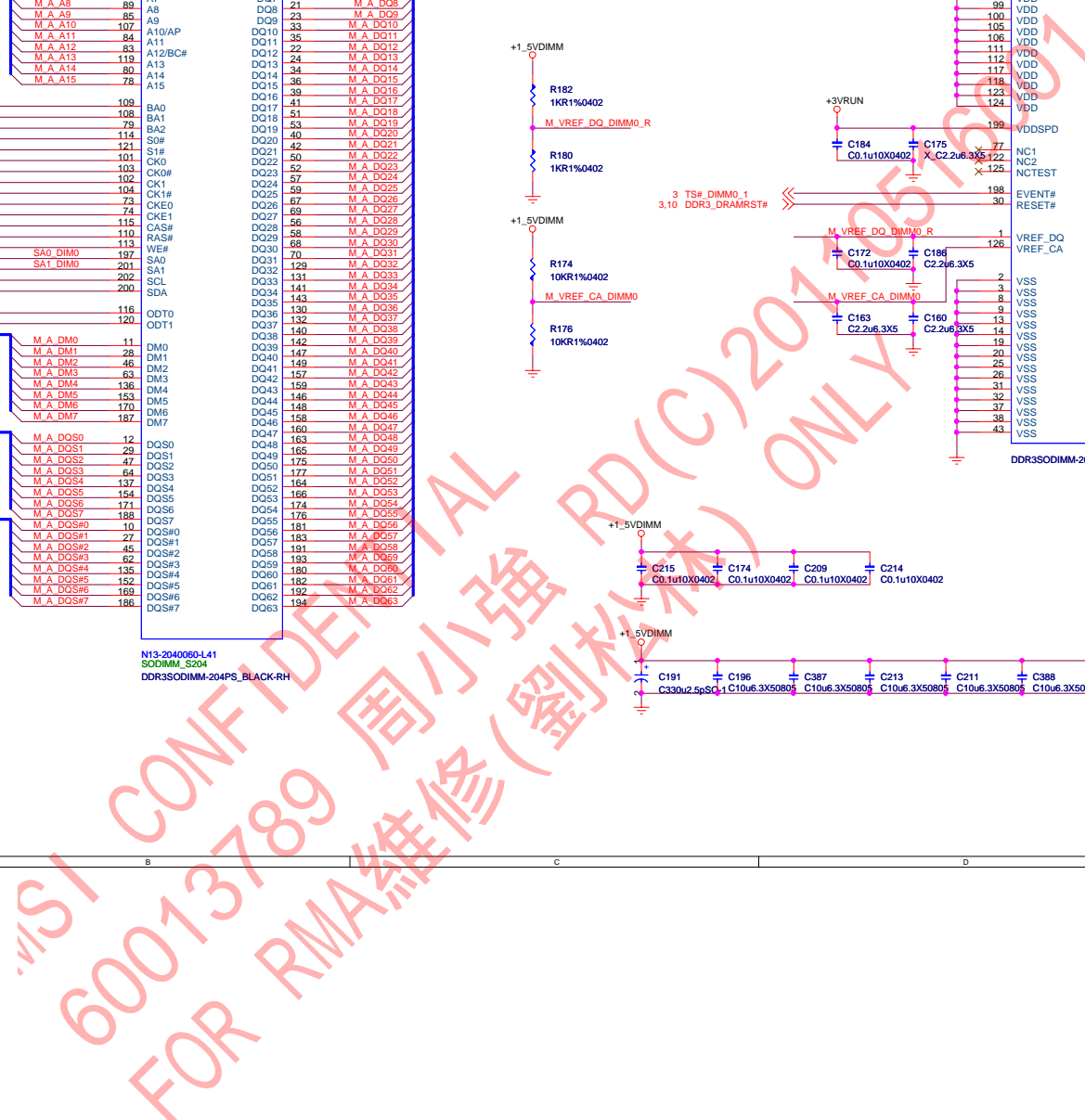
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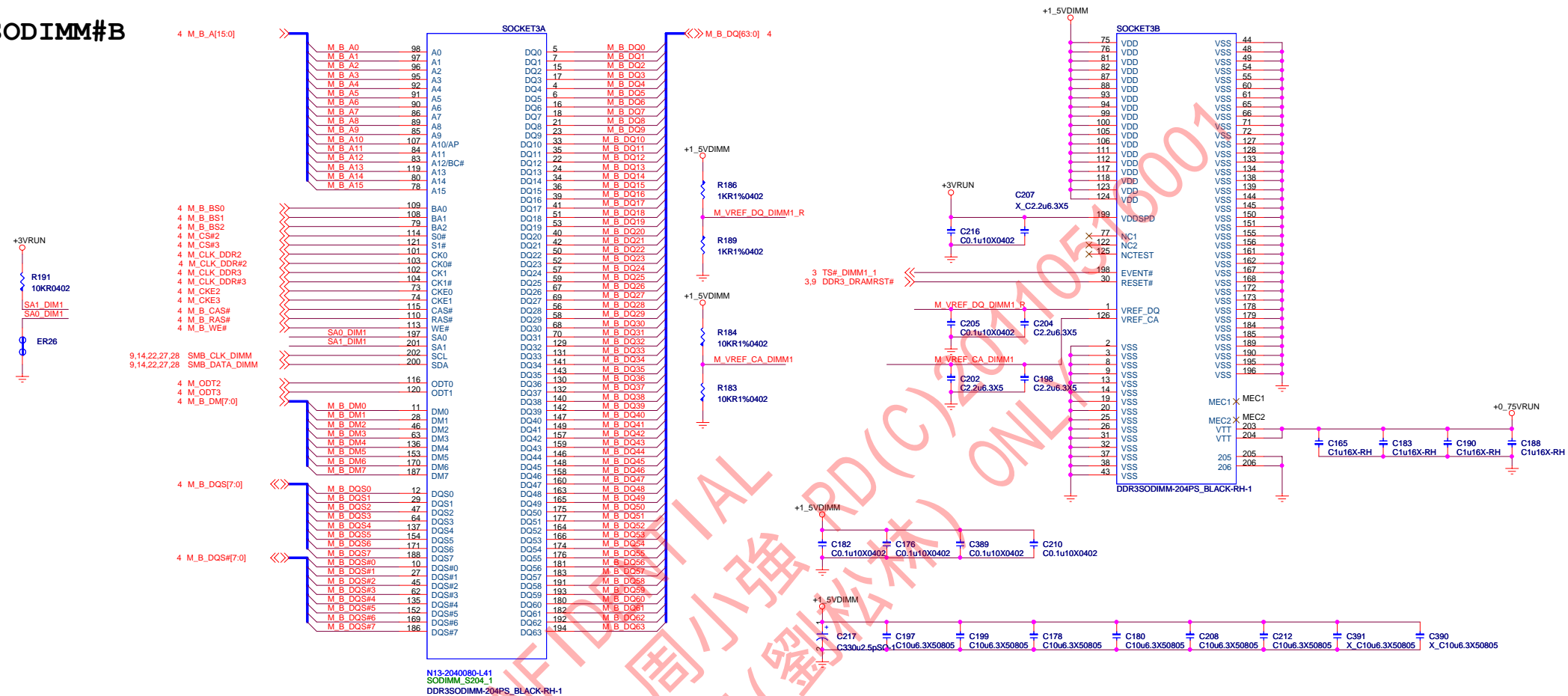
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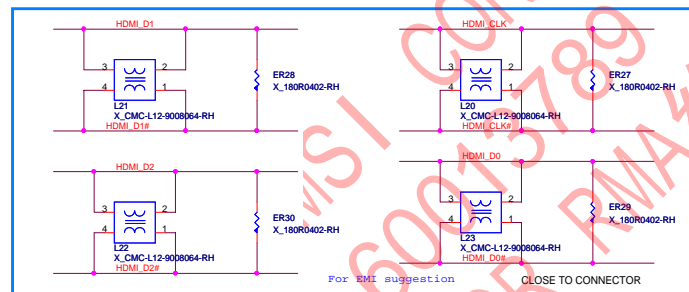
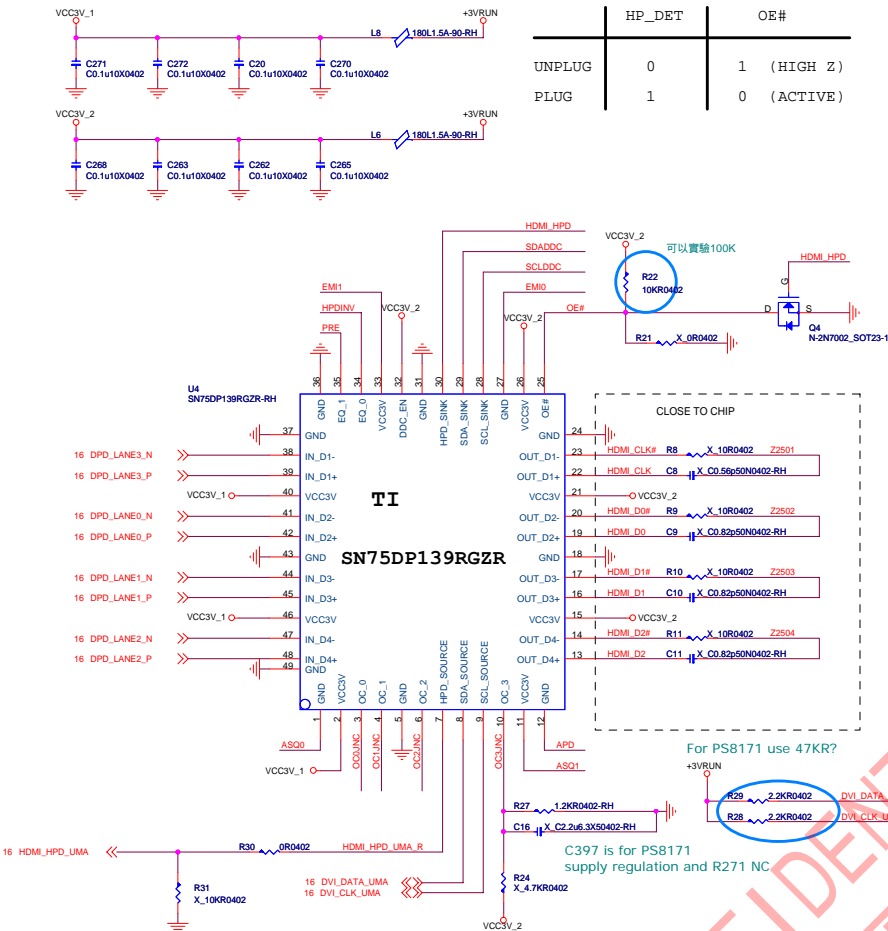


SODIMM#B

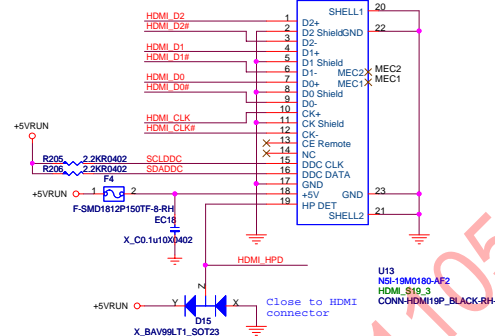


	MICRO-STAR INT'L CO.,LTD.	
Title DDR3 SODIMM1		
Size Custom	Document Number <div style="font-size: 1.2em; font-weight: bold; text-align: center;">MS-1681</div>	Rev 10
Date: Thursday, December 17, 2009 Sheet 10 of 45		

HDMI Switch

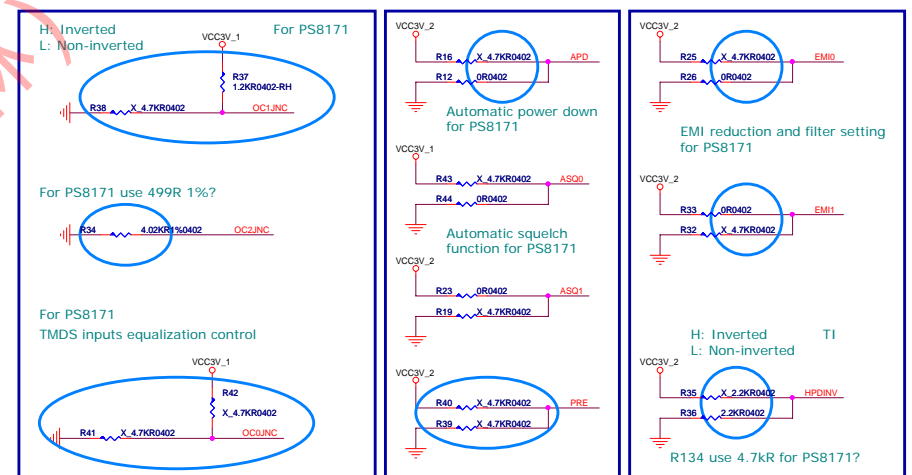


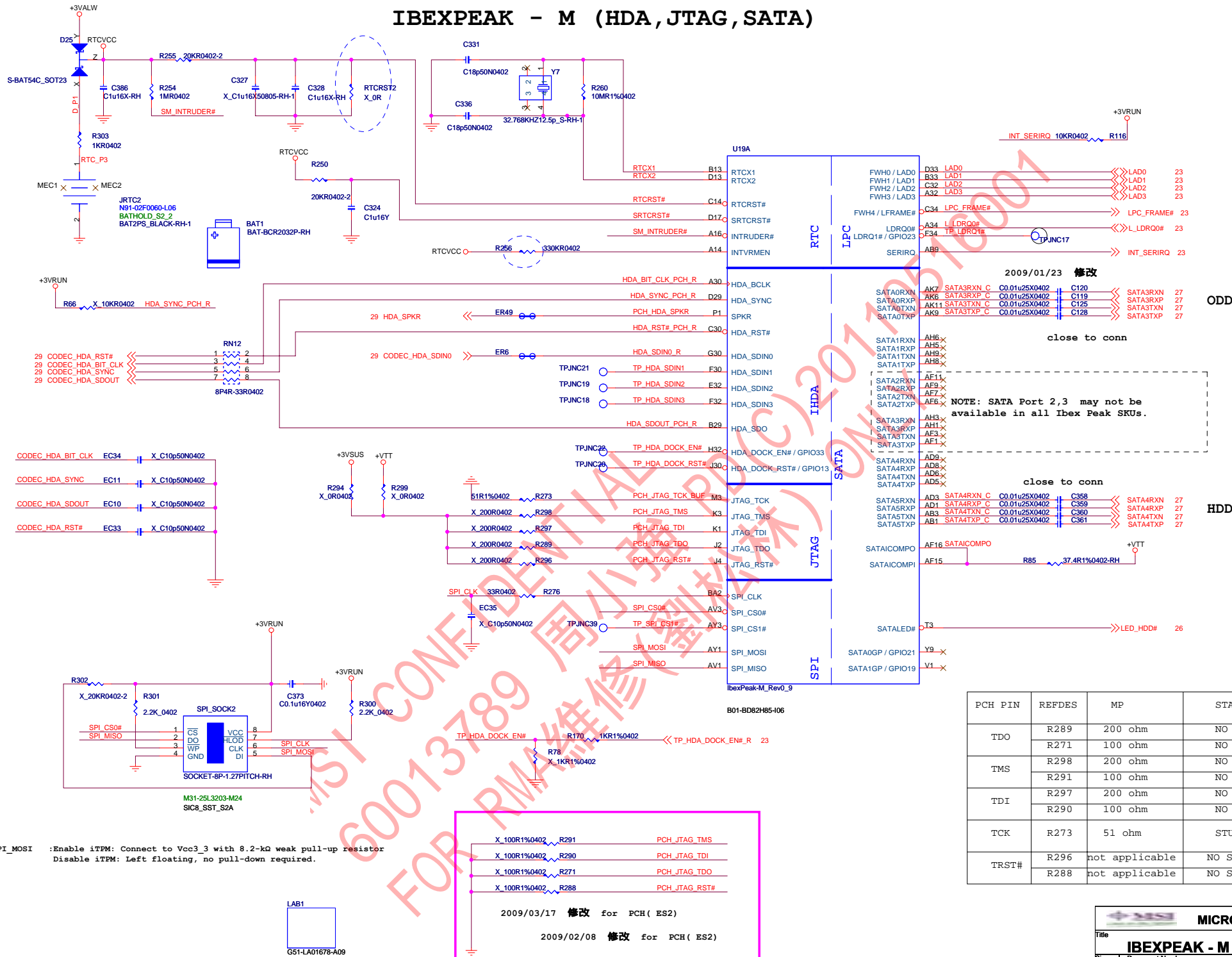
HDMI connector



SN75DP139	PS8171	Pin no.
Floating	TMDS inputs equalization control (internal pull-down~500KΩ) PEQ = LOW: Mid level EQ (Default) PEQ = HIGH: High level EQ PEQ = MID: Low level EQ	Pin 3
High	(Internal pull down~500KΩ) PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output PIO = High: HPD= HPD_SINK# (inverted HPD) @ 0.3V	Pin 4
GND	[ASQ1,ASQ0] = HL: No automatic squelch (internal pull down~500KΩ) LL: Automatic squelch enable, Level = 120mVpp, default timer LH: Automatic squelch enable, Level = 100mVpp, default timer HH: Automatic squelch enable, Level = 80mVpp, default timer ML: Automatic squelch enable, Level = 120mVpp, extended timer MH: Automatic squelch enable, Level = 100mVpp, extended timer LM: Automatic squelch enable, Level = 80mVpp, extended timer HM: Reserved MM: Reserved	Pin 1 Pin 11
4.85K to GND	499R to GND	Pin 6
GND	Automatic power down management (Internal pull up~500KΩ) APD = LOW: Automatic power down disable APD = HIGH: Automatic power down enable APD = MID: Reserved	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND	EMI reduction and filter setting. (EMI1 internal pull up~500KΩ; EMI0 internal pull down~500KΩ) (EMI1,EMI0) = HL: No EMI reduction EMIO = HIGH: Reduced rise/fall time MID: Reduced rise/fall time, 2nd EMI1 = LOW: EMI filter setting 1 MID: Reserved	Pin 27 Pin 33
Note2	DDC Active Buffer enable and setting (internal pull-down~500KΩ) DDCBUF = LOW: No DDC active buffer, passive DDC level shifting DDCBUF = HIGH: Active DDC buffer enable, setting 1 DDCBUF = MID: Active DDC buffer enable, setting 2	Pin 34
Floating	TMDS output driver pre-emphasis level setting (internal pull down~500KΩ) PRE = LOW No pre-emphasis PRE = HIGH: Low level pre-emphasis is added PRE = MID: High level pre-emphasis is added	Pin 35

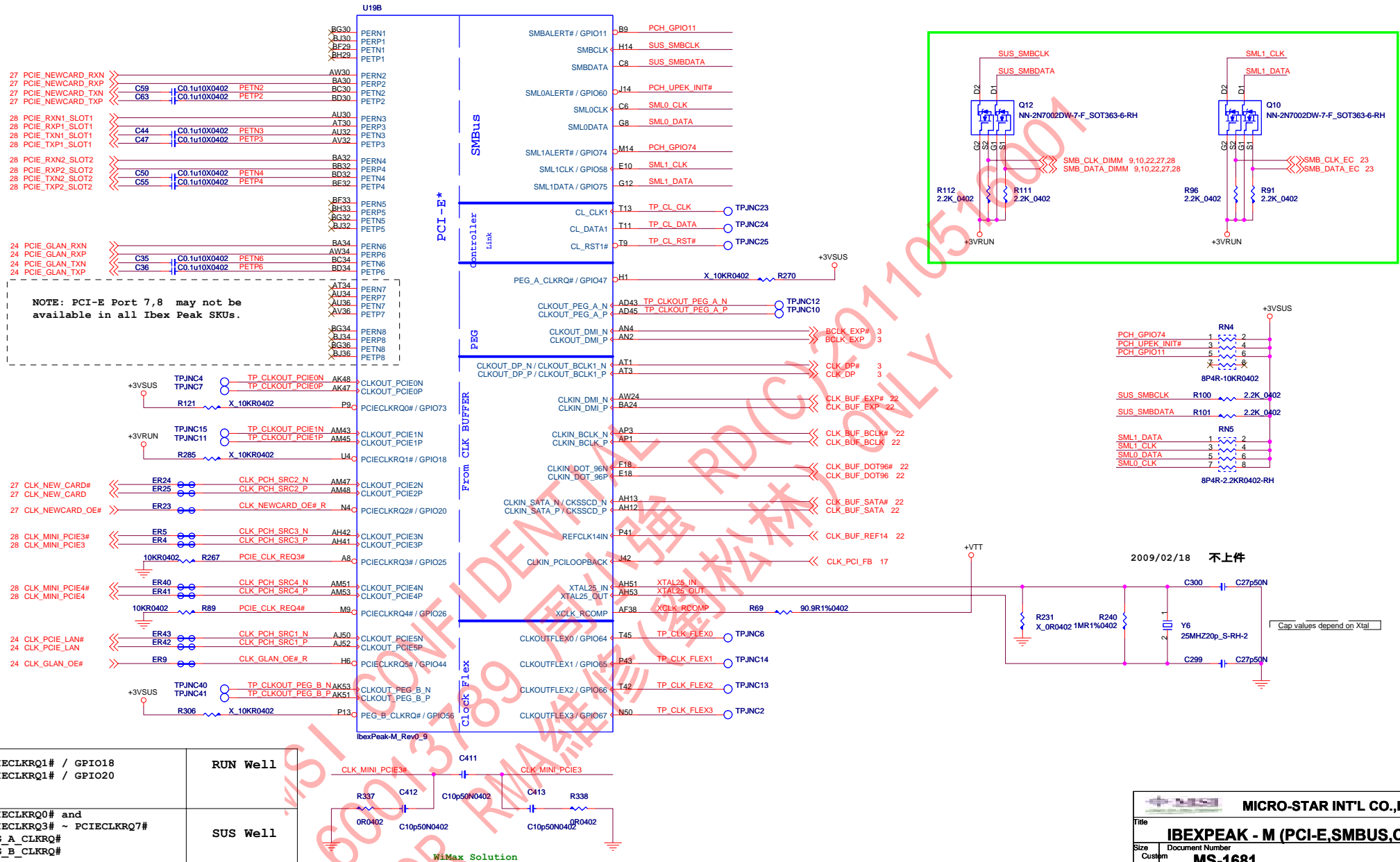
Note2: High is HPD logic inverted, Low is HPD logic non-inverted



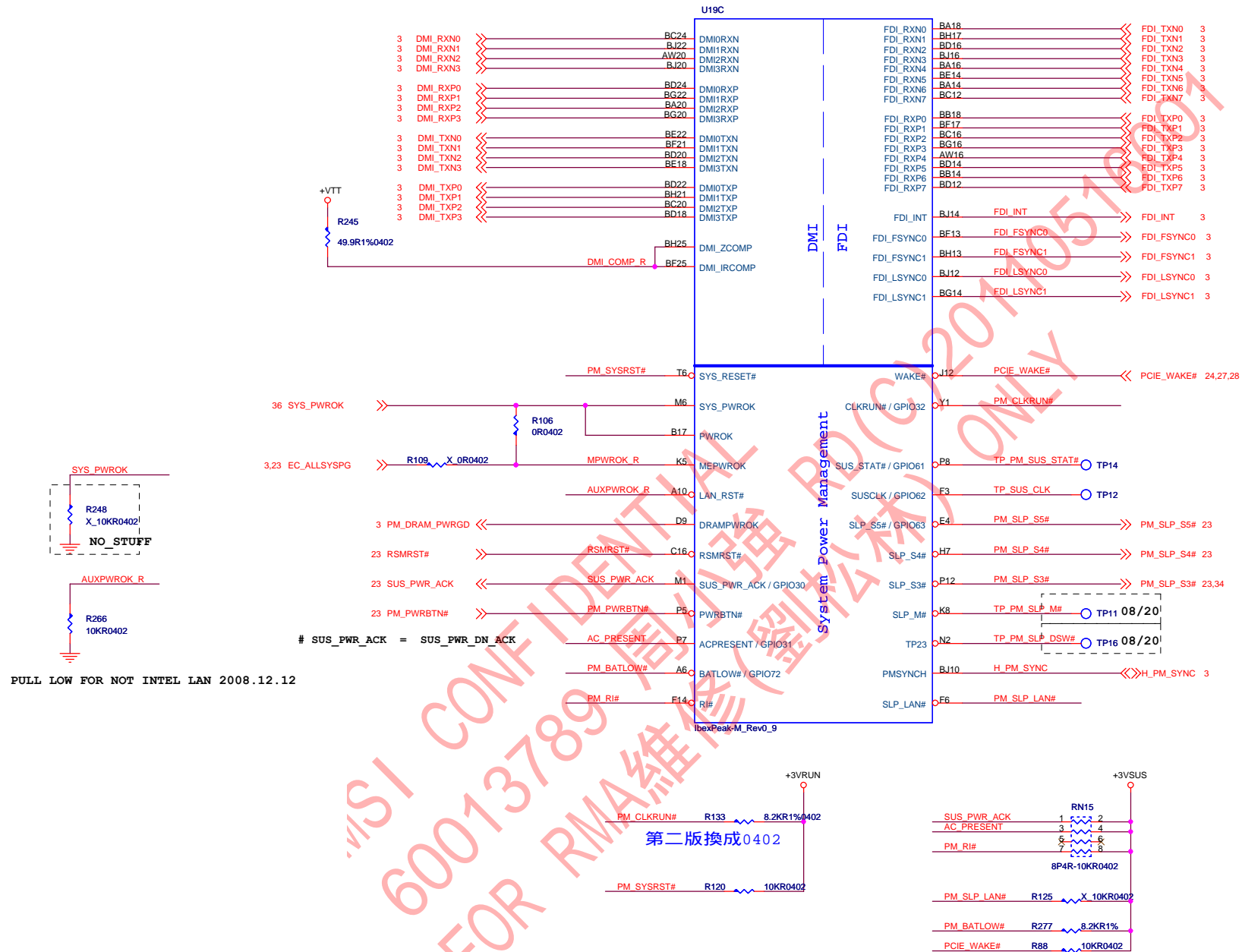
IBEXPEAK - M (HDA, JTAG, SATA)

PCH PIN	REFDES	MP	STATE
TDO	R289	200 ohm	NO STUFF
	R271	100 ohm	NO STUFF
TMS	R298	200 ohm	NO STUFF
	R291	100 ohm	NO STUFF
TDI	R297	200 ohm	NO STUFF
	R290	100 ohm	NO STUFF
TCK	R273	51 ohm	STUFF
TRST#	R296	not applicable	NO STUFF
	R288	not applicable	NO STUFF

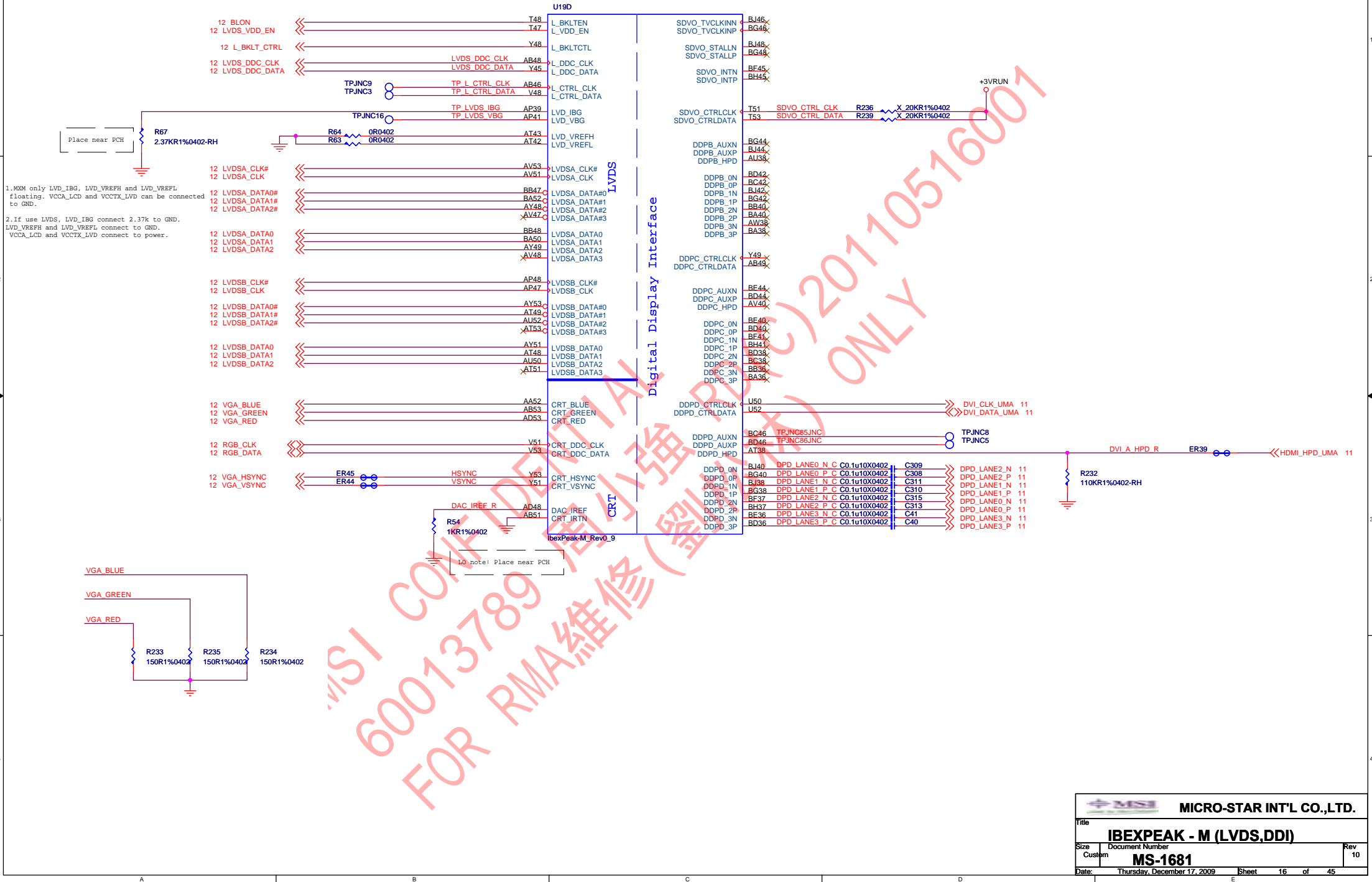
IBEXPEAK - M (PCI-E, SMBUS, CLK)



IBEXPEAK - M (DMI, FDI, GPIO)



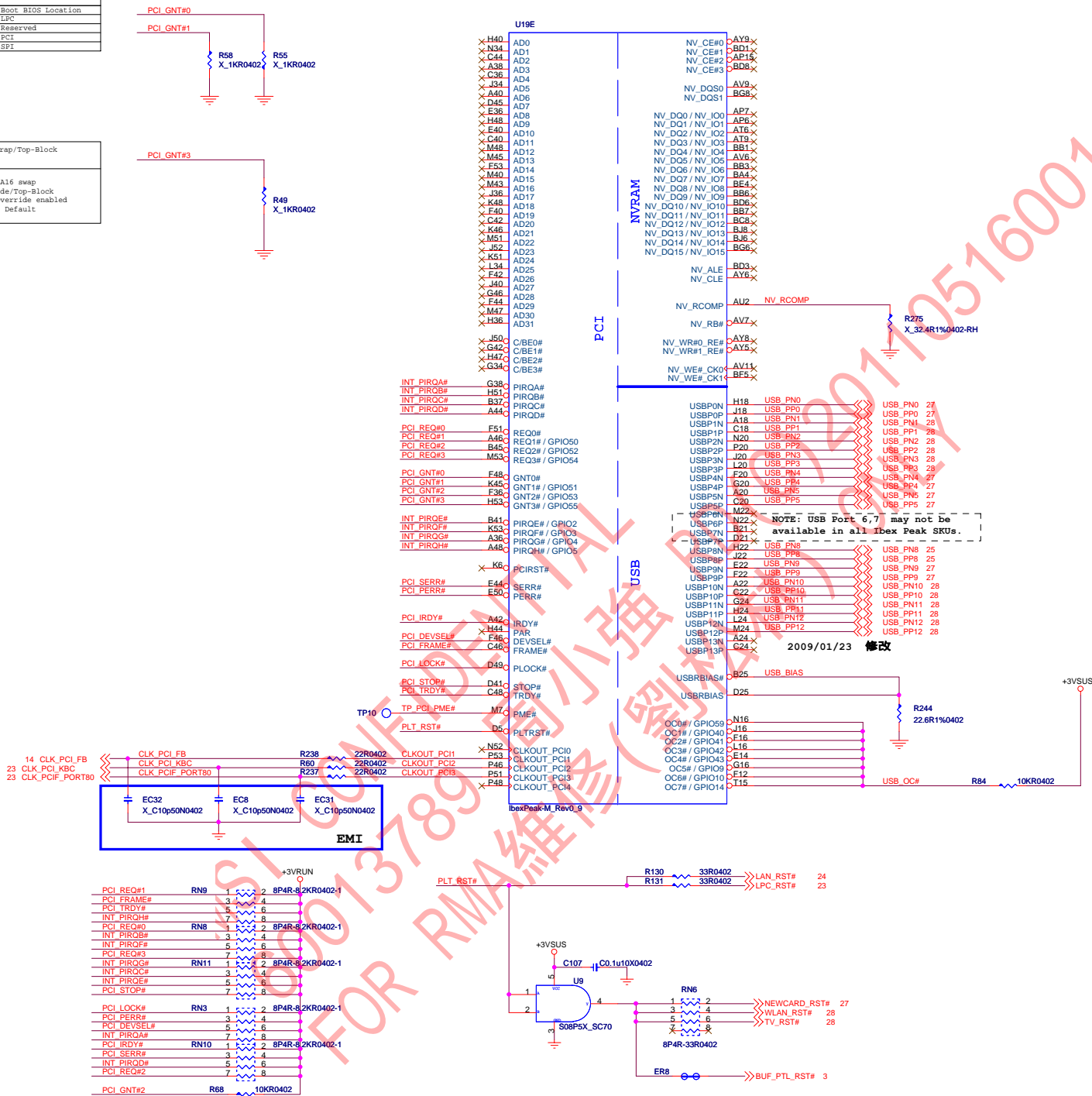
IBEXPEAK - M (LVDS,DDI)



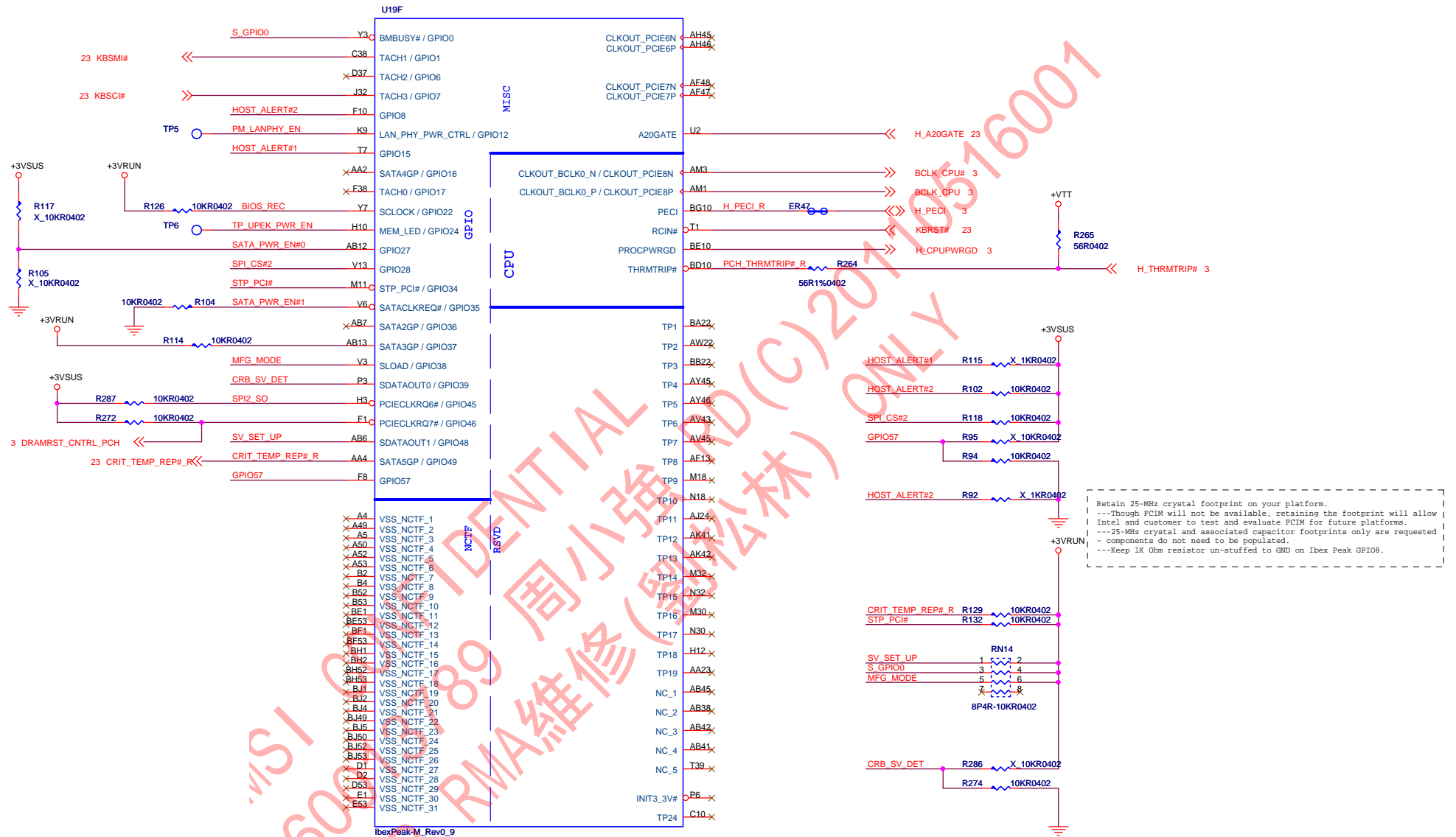
IBEXPEAK - M (PCI,USB,NVRAM)

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI

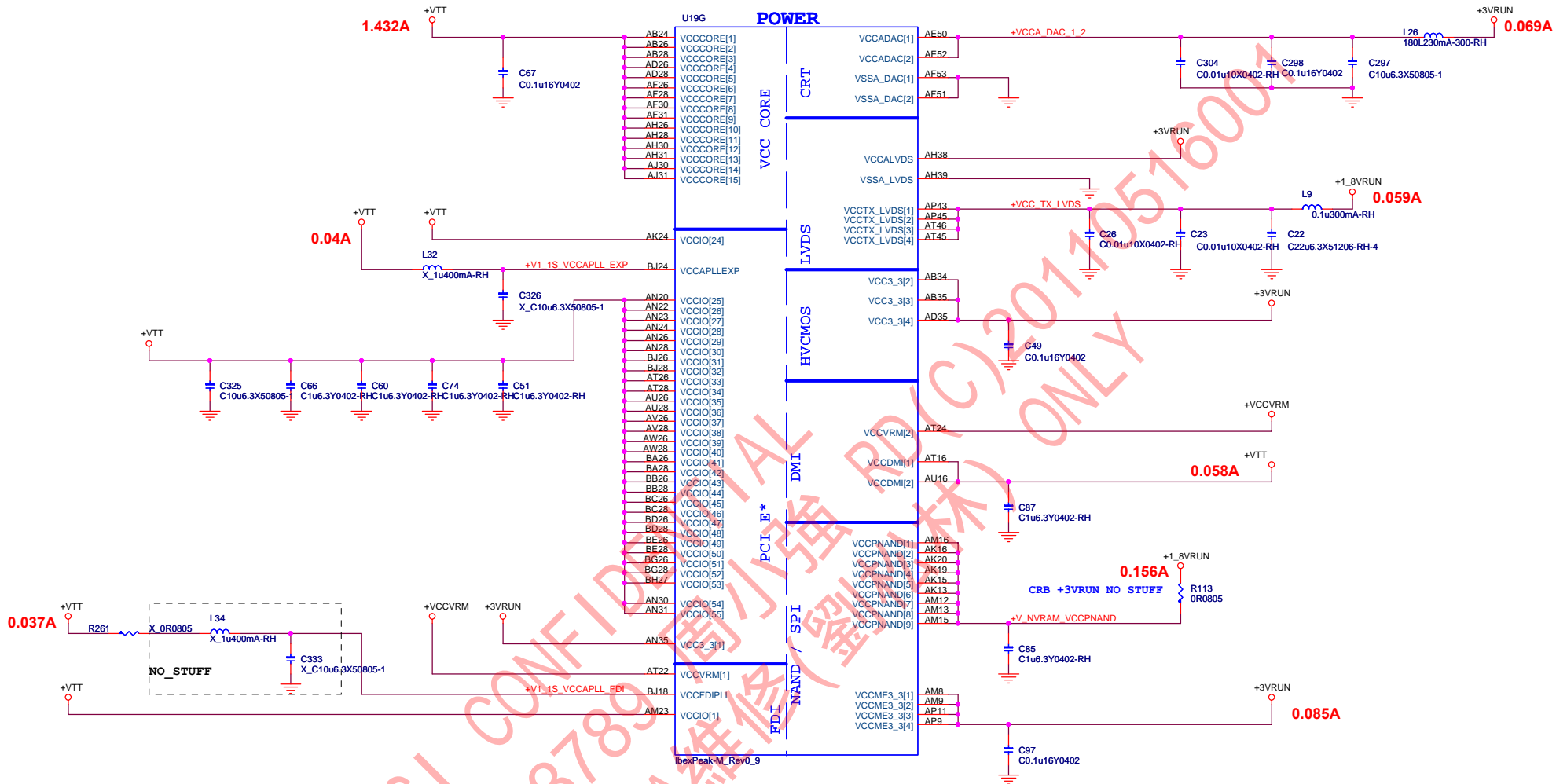
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



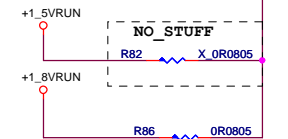
IBEXPEAK - M (GPIO,VSS_NCTF,RSVD)



IBEXPEAK - M (POWER)

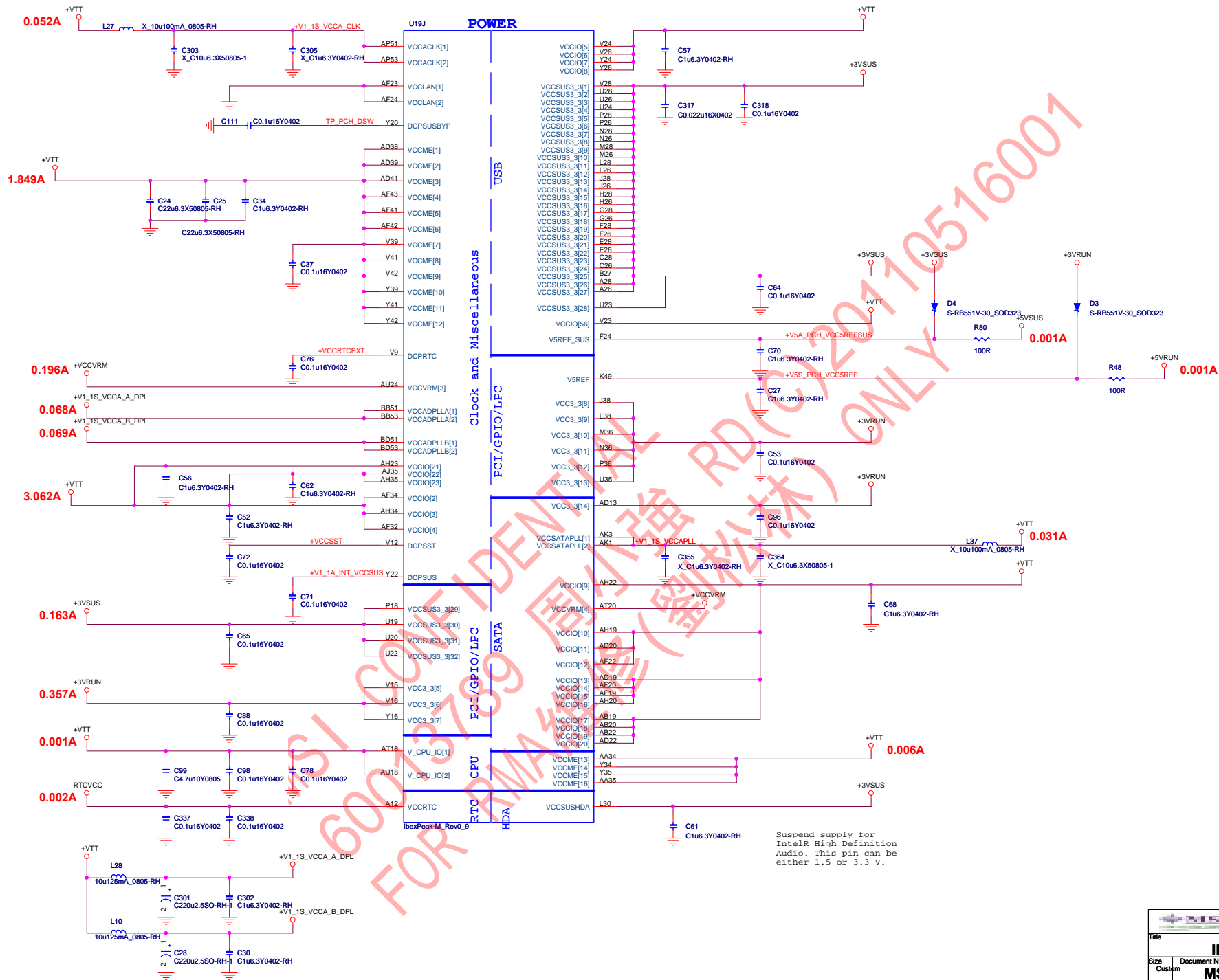


The VCCVPM rail (1.8 V/1.5 V) powers an internal voltage regulator module (VRM) that regulates clean 1.05-V voltage supply for analog rails (VCCAClk, VccapllEXP, VCCFDIPLL, and VCCSATAPLL). This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. VCCVPM is enabled by default via internal pull up to GPIO27, therefore GPIO27 should be left as No Connect. The following diagram shows implementation details on how to enable and disable VccVRM.

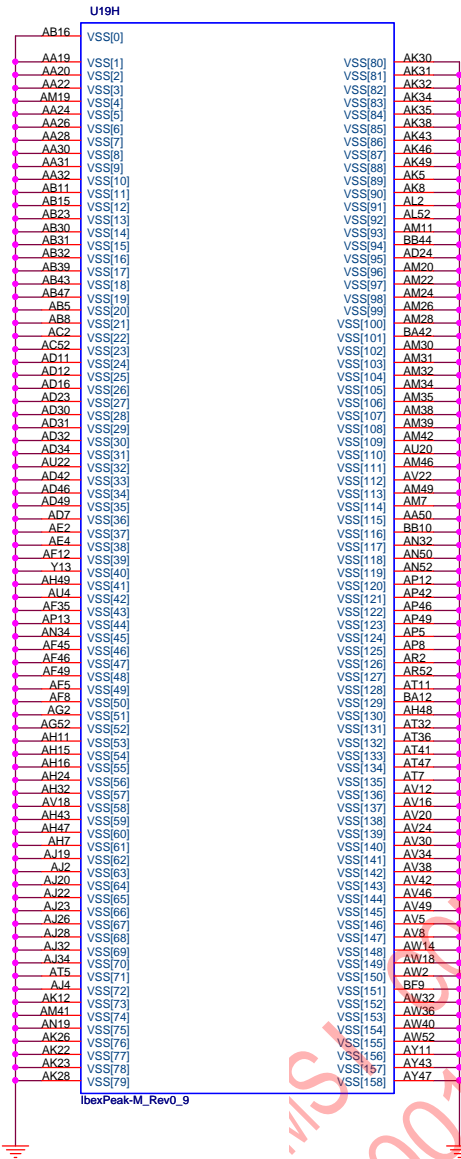


VccLAN may be grounded if Intel LAN is disabled.

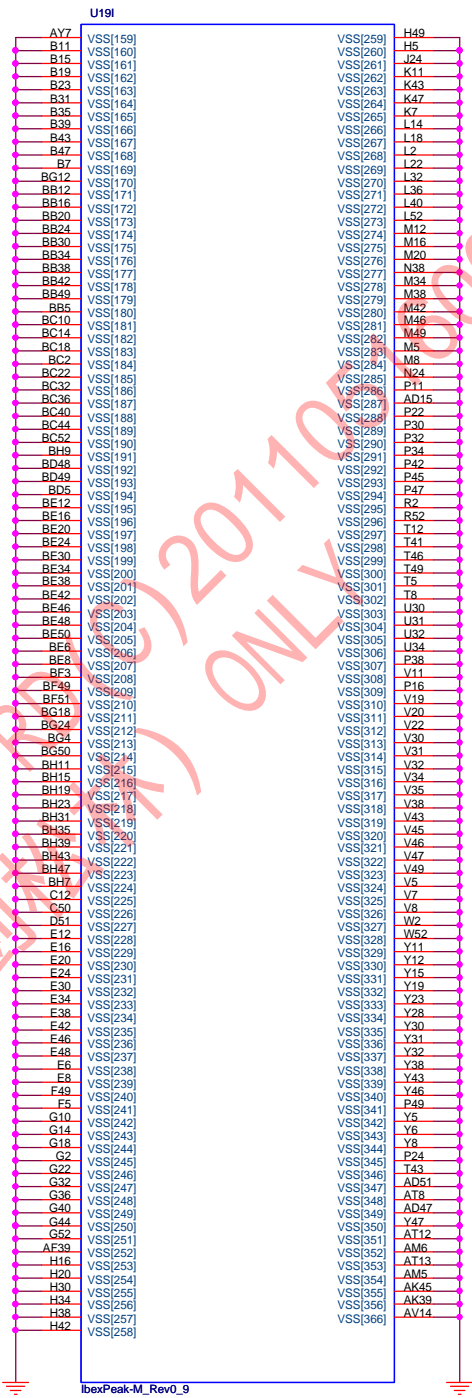
IBEXPEAK - M (POWER)




IBEXPEAK - M (GND)

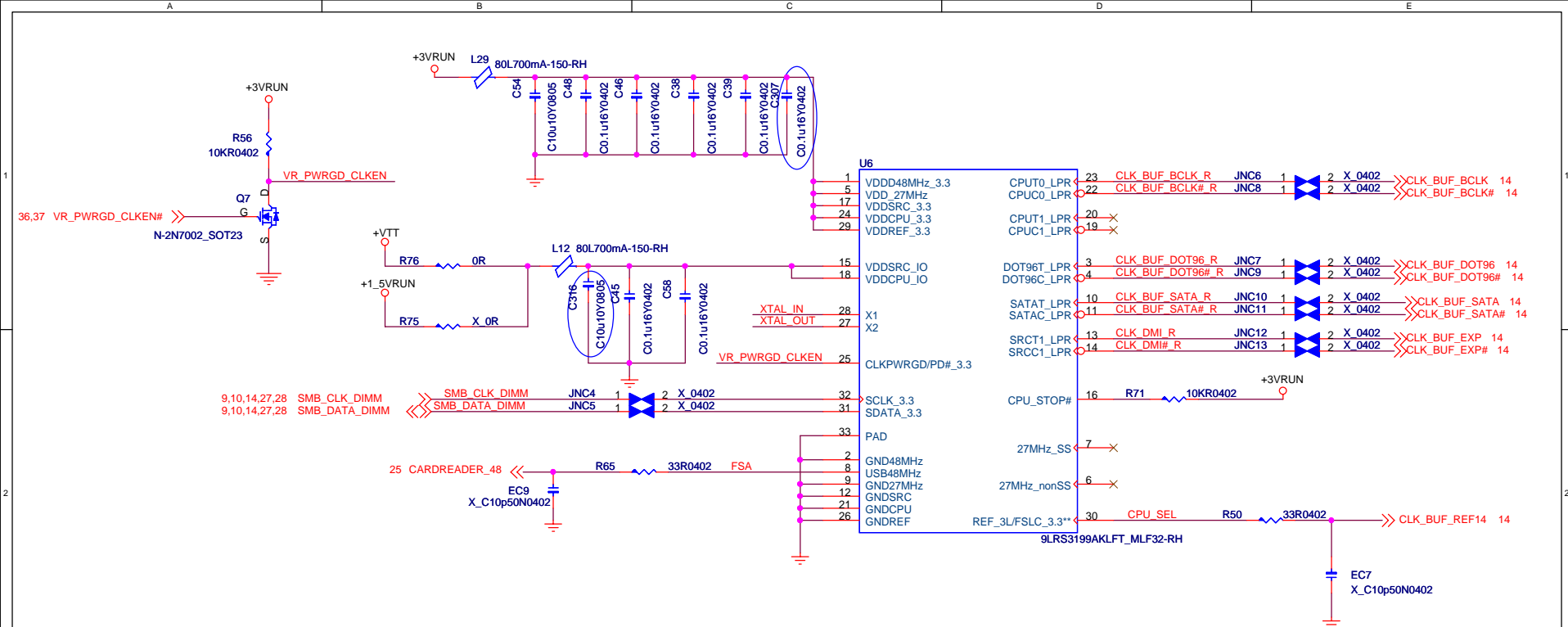


ibexPeak-M_Rev0_9



ibexPeak-M_Rev0_9

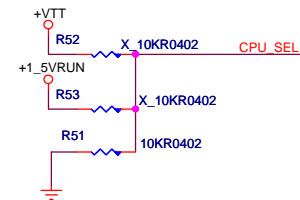
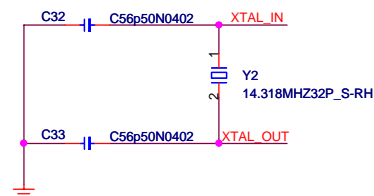
		MICRO-STAR INT'L CO.,LTD.	
Title			
IBEXPEAK - M (GND)			
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For CPU frequency select (133MHz)

Capacity select

If LC=20pf C708/C709=33pf
If LC=32pf C708/C709=56pf



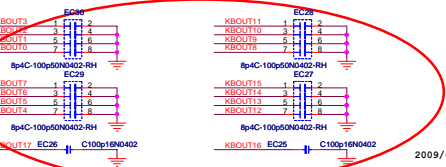
CPU_SEL	CPU0	CPU1
0(Default)	133MHz	133MHz
1(1.05~1.5V)	100MHz	100MHz

Co-Lay Note:

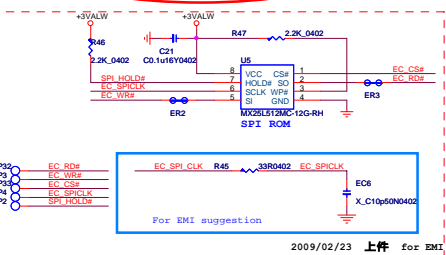
For IDT IC9IRS3199
R598,R599,R600=10Kohm

For Silago SLG8SP587
R598,R599,R600=4.7Kohm

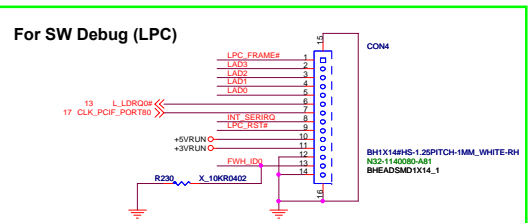
BATT_DACCHG 預留不接地



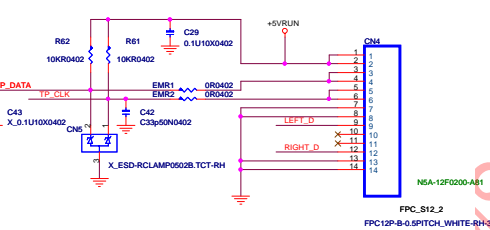
2009/02/23 上件 for EMI



2009/02/23 上件 for EMI



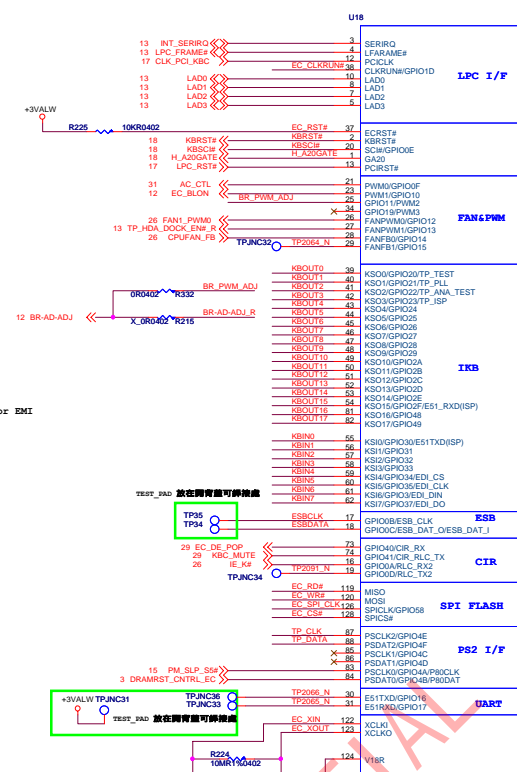
Touch Pad



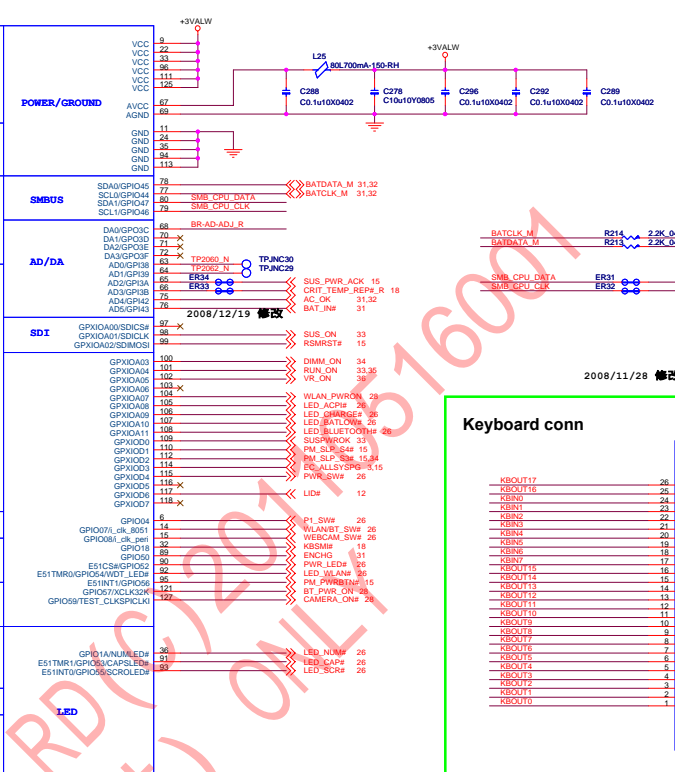
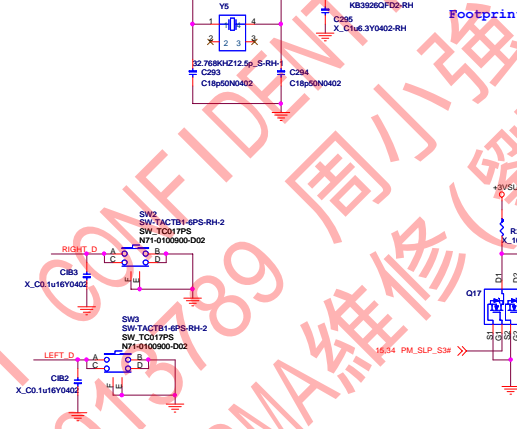
N5A-12F0200-A81

FPC_S12_2

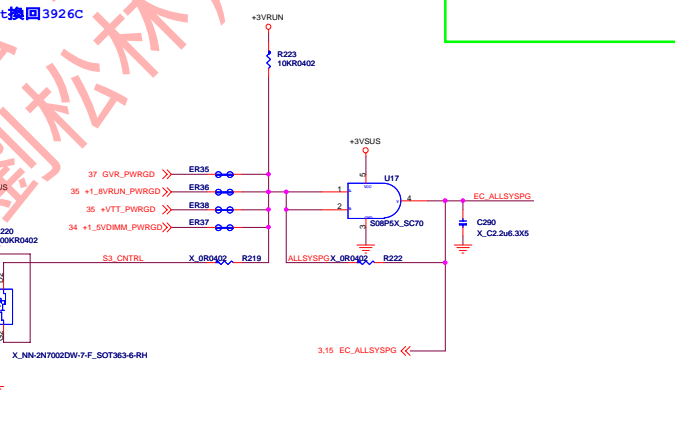
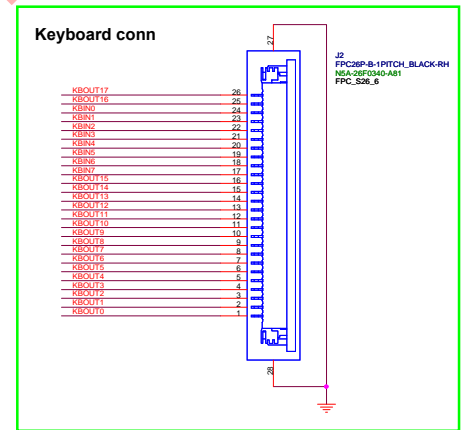
3-0.5PITCH_WHITE-RH-3



Footprint 換回 3926C



2008/11/28 修改

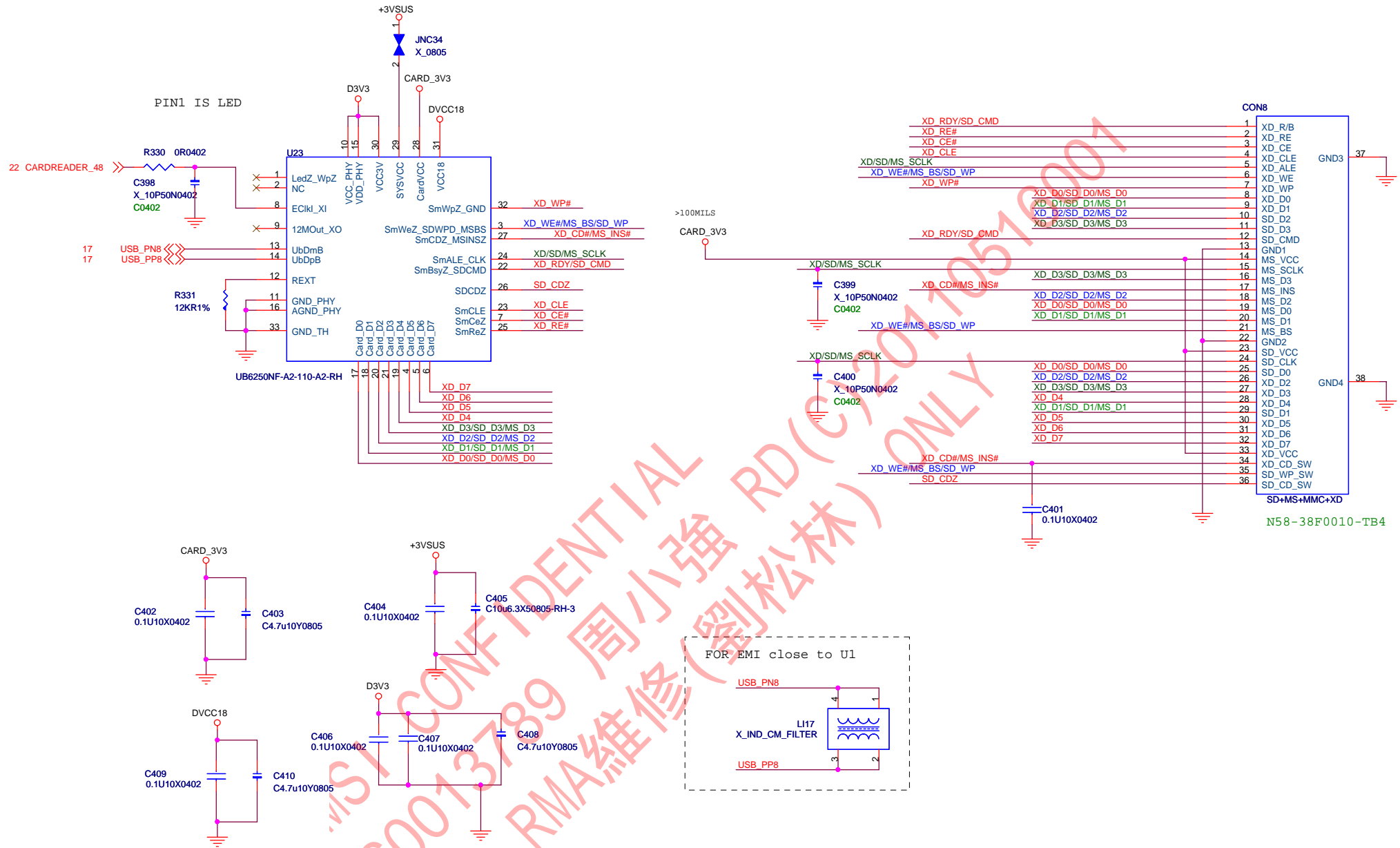


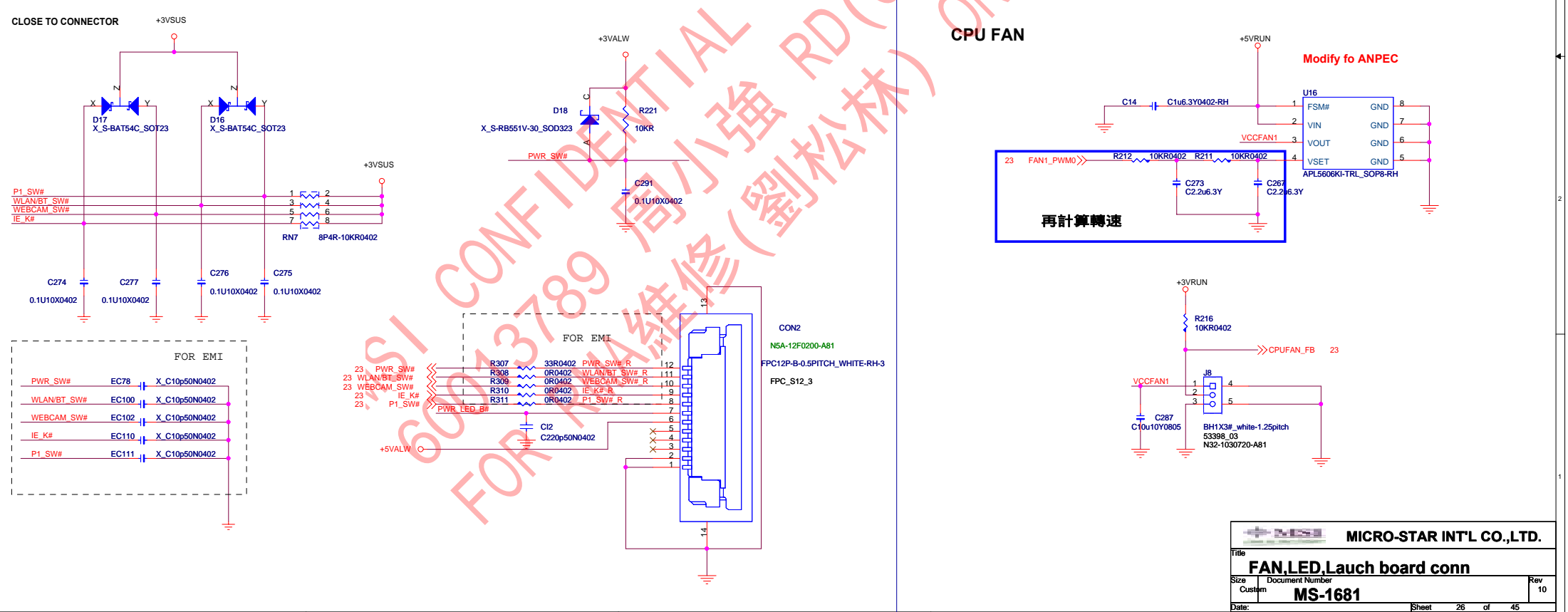
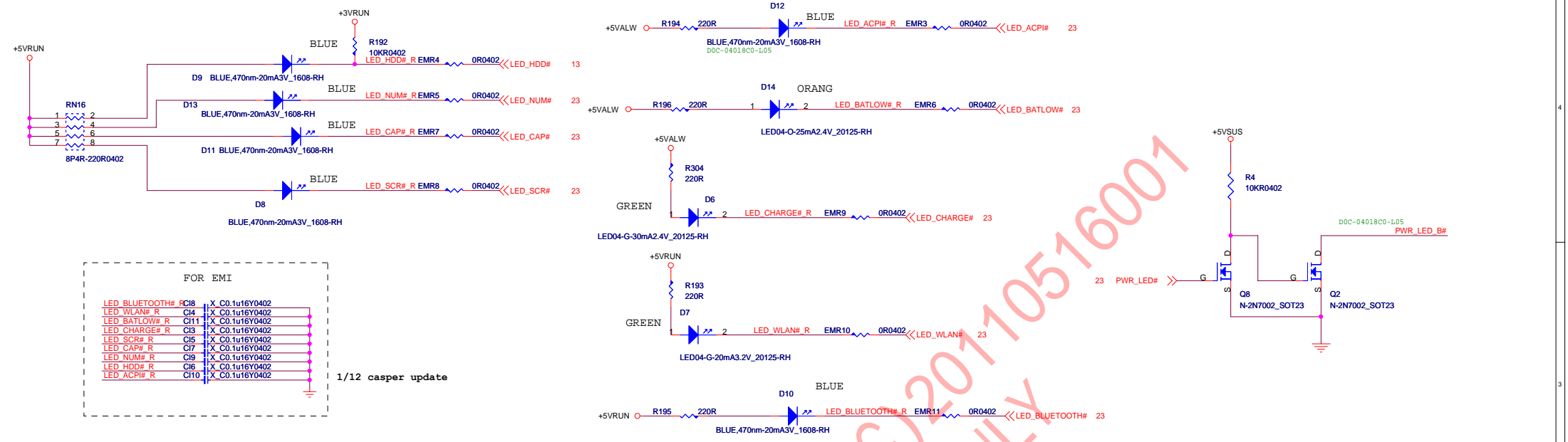
- 4

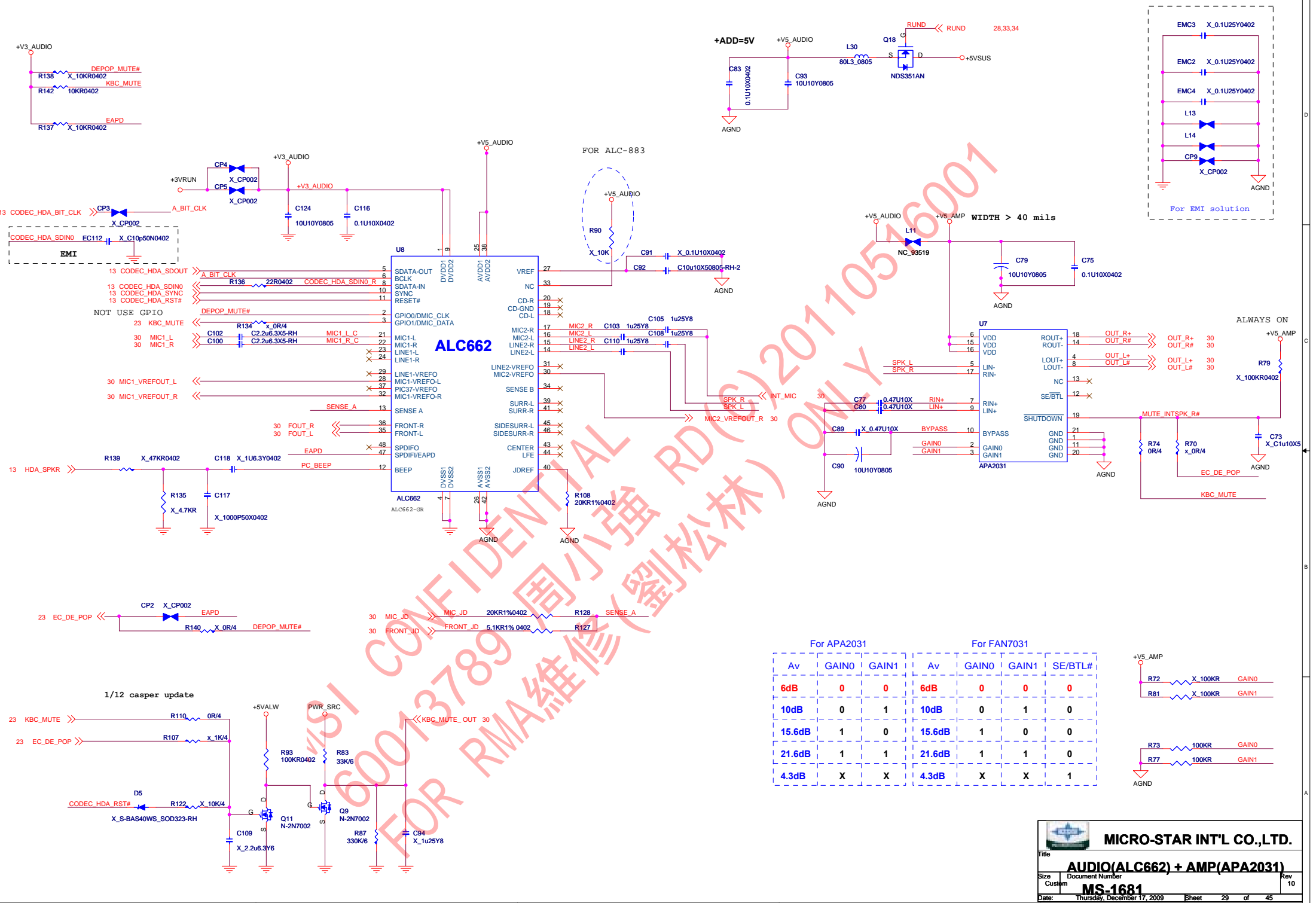


3

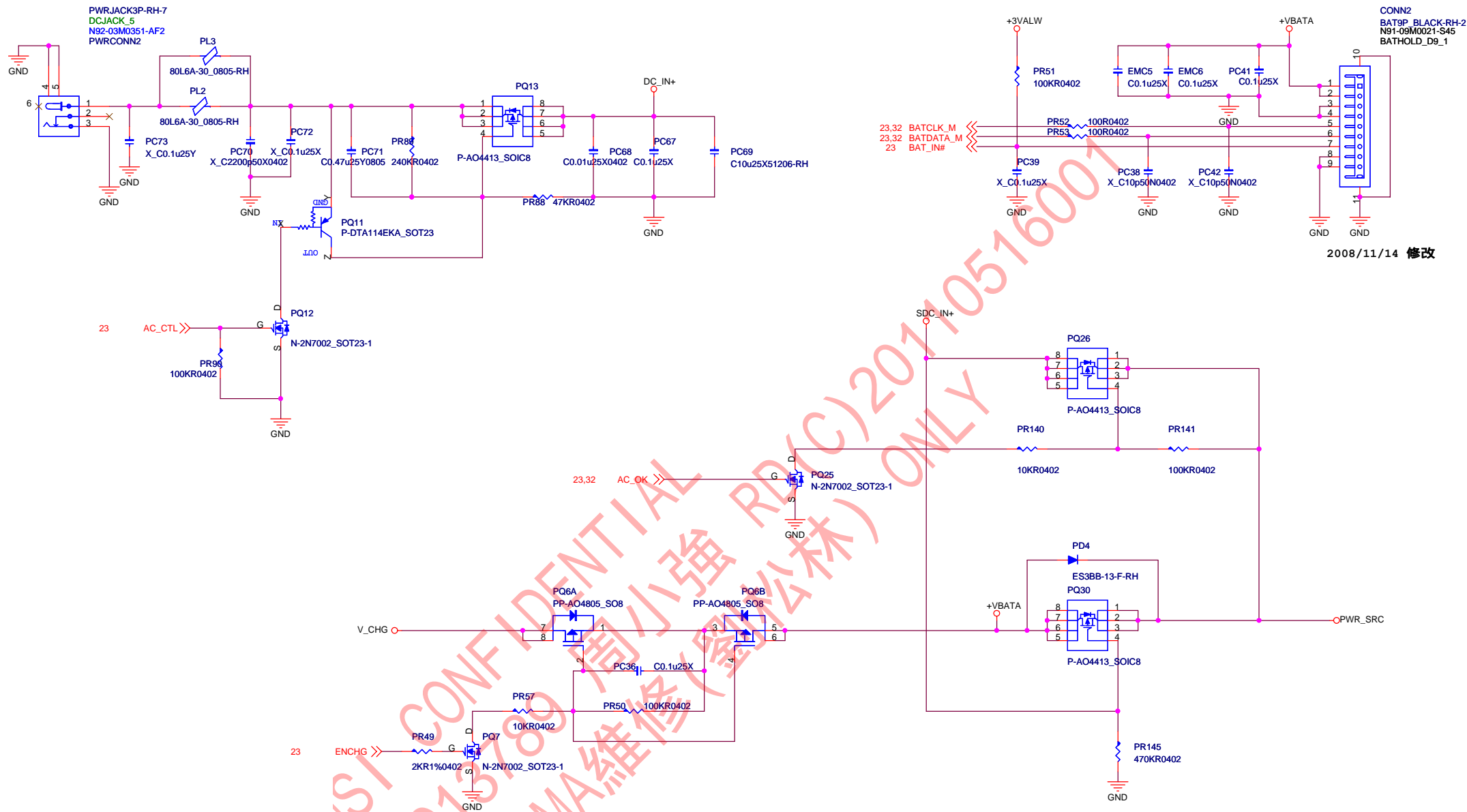
4







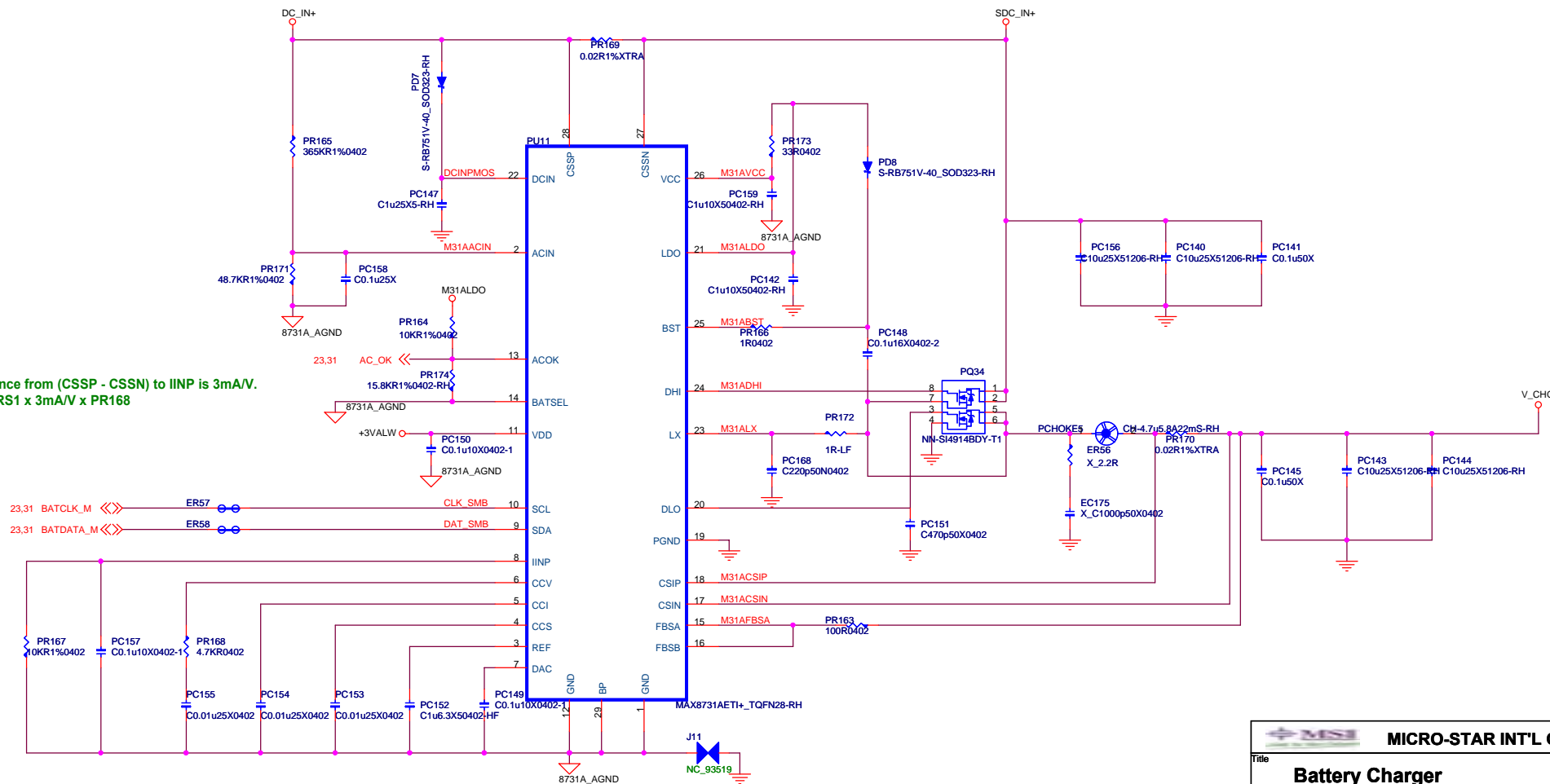
For APA2031				For FAN7031			
Av	GAIN0	GAIN1		Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0		6dB	0	0	0
10dB	0	1		10dB	0	1	0
15.6dB	1	0		15.6dB	1	0	0
21.6dB	1	1		21.6dB	1	1	0
4.3dB	X	X		4.3dB	X	X	1



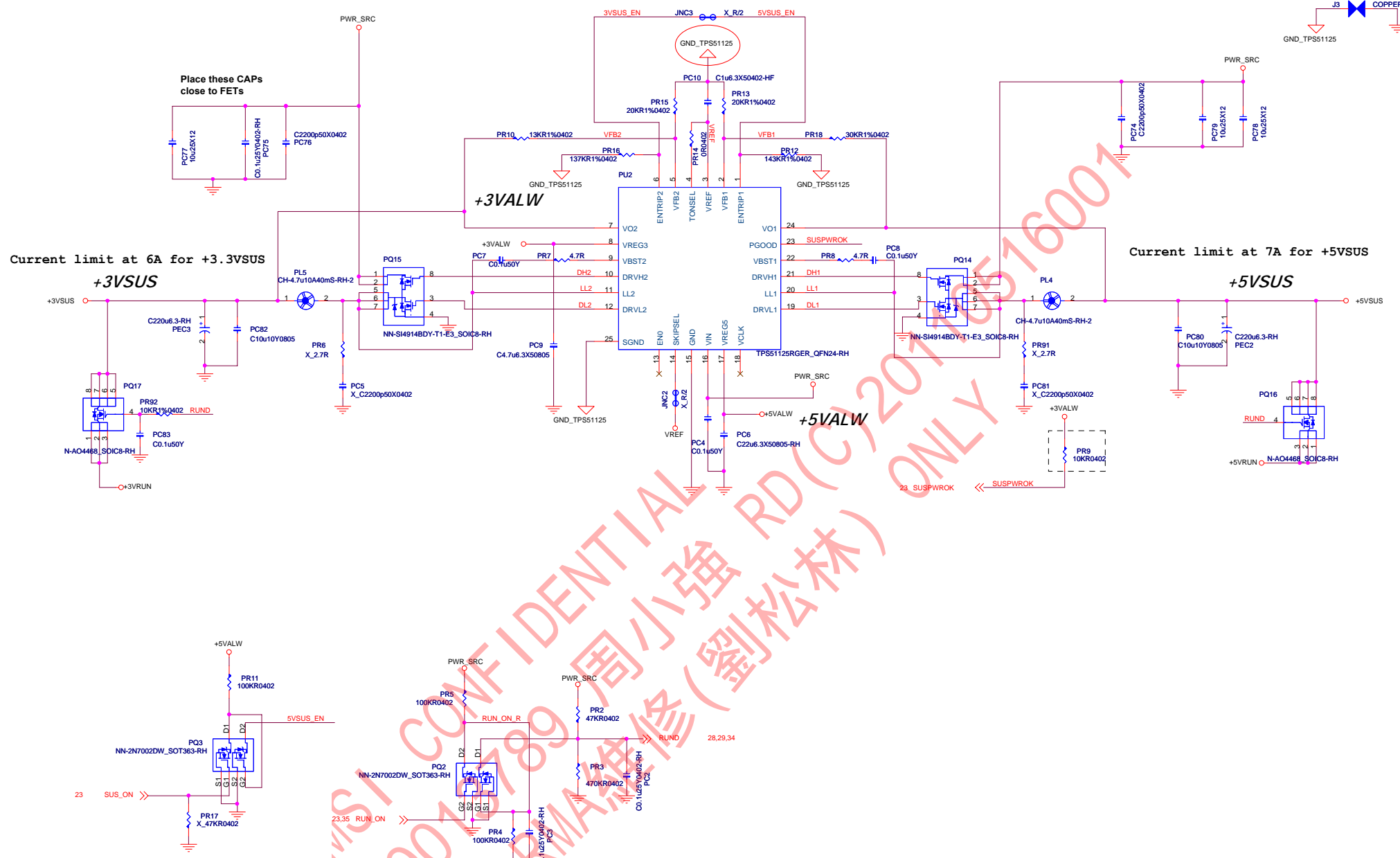
MSI MICRO-STAR INT'L CO.,LTD.		
Title		
Battery Select		
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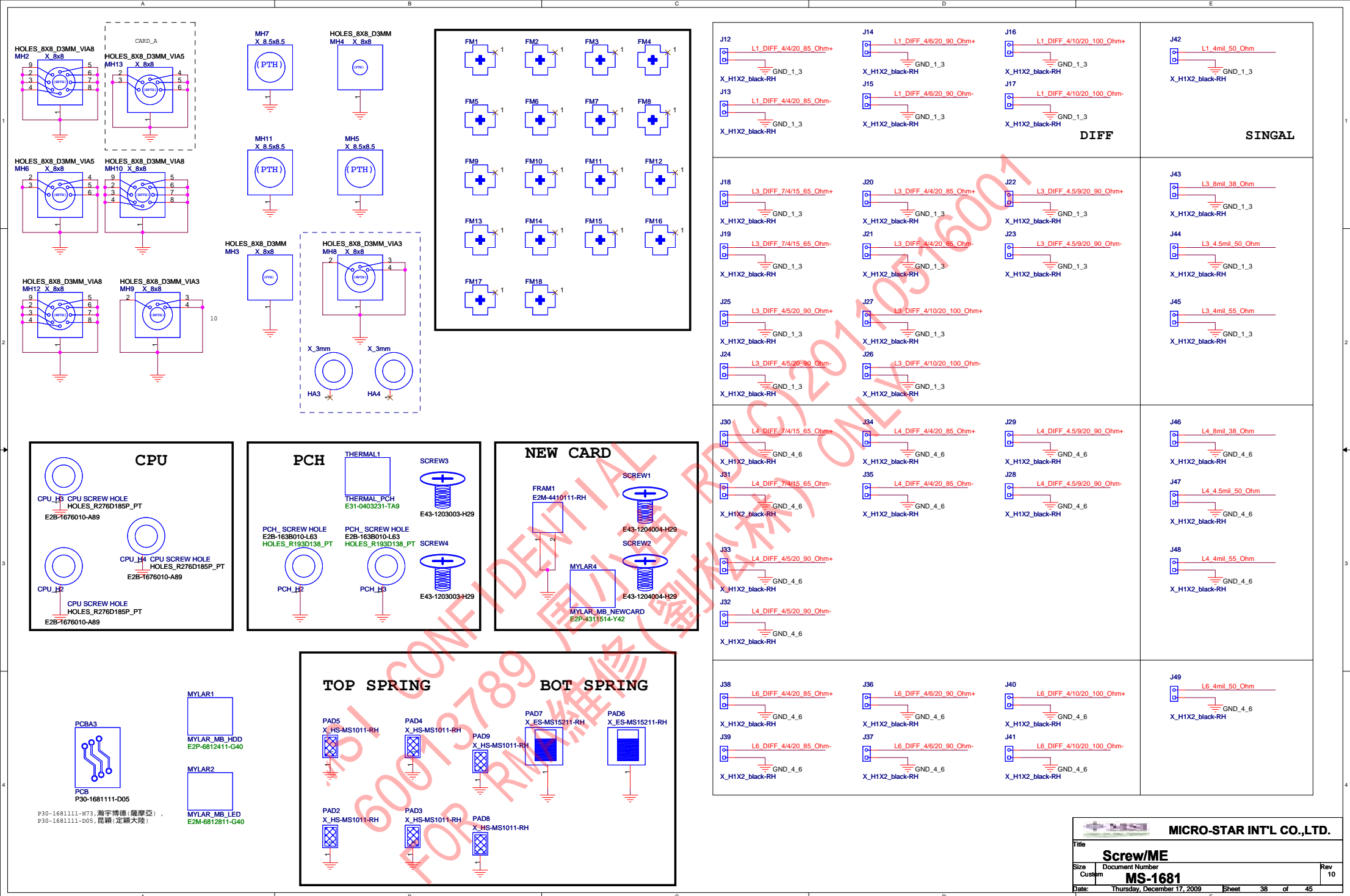
Adapter= 65W
Adapter input voltage set 19 Voltage

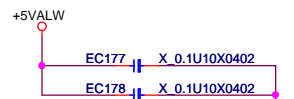
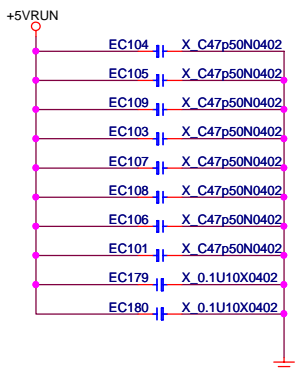
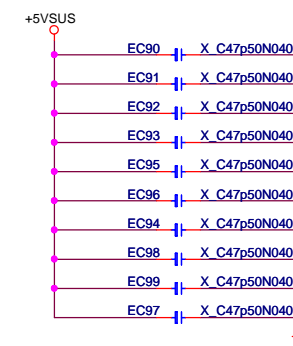
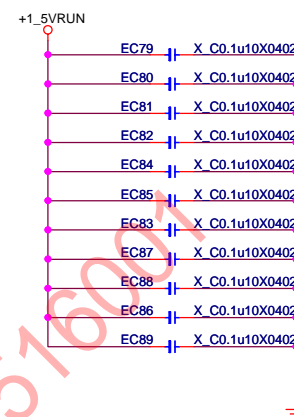
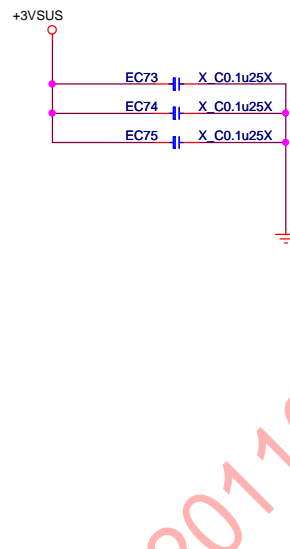
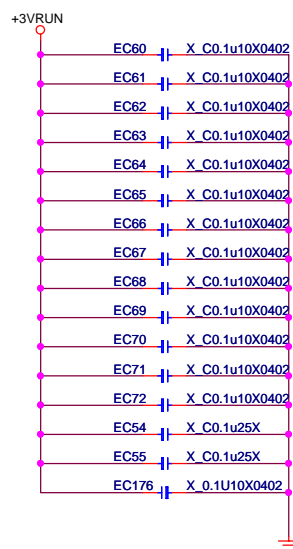
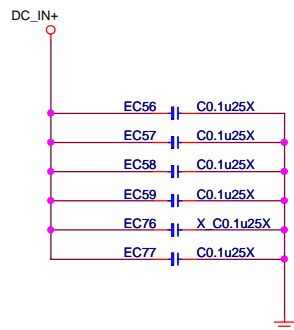
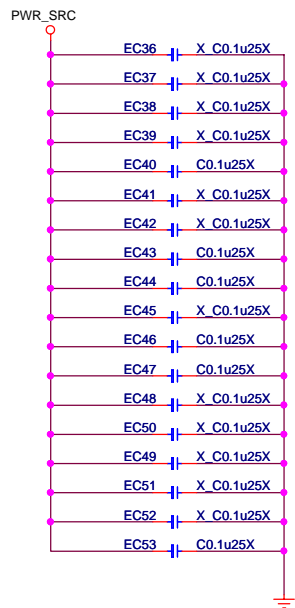
IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINPUT \times RS1 \times 3mA/V \times PR168$



MICRO-STAR INT'L CO.,LTD.			
Title			
Battery Charger			
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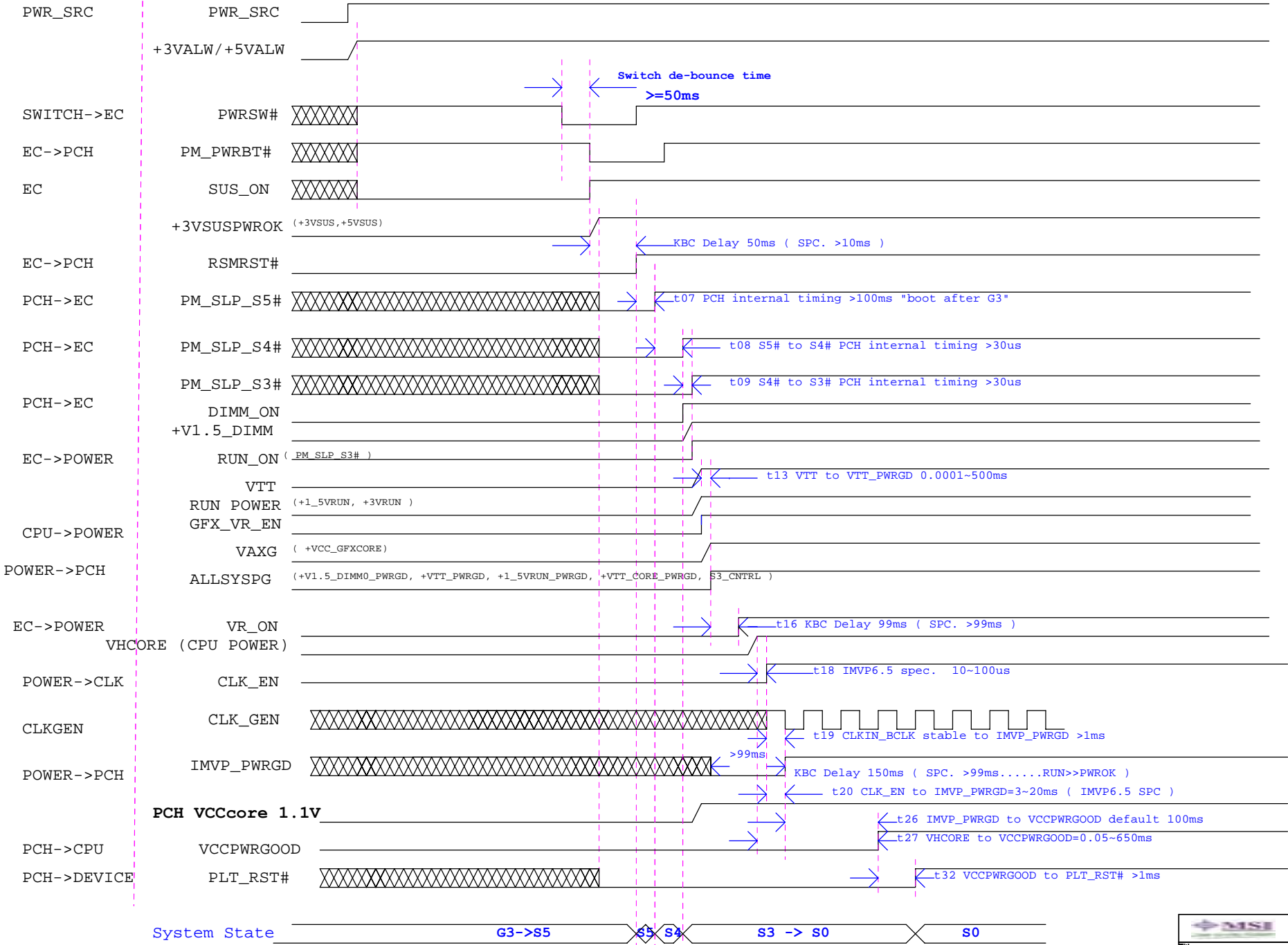




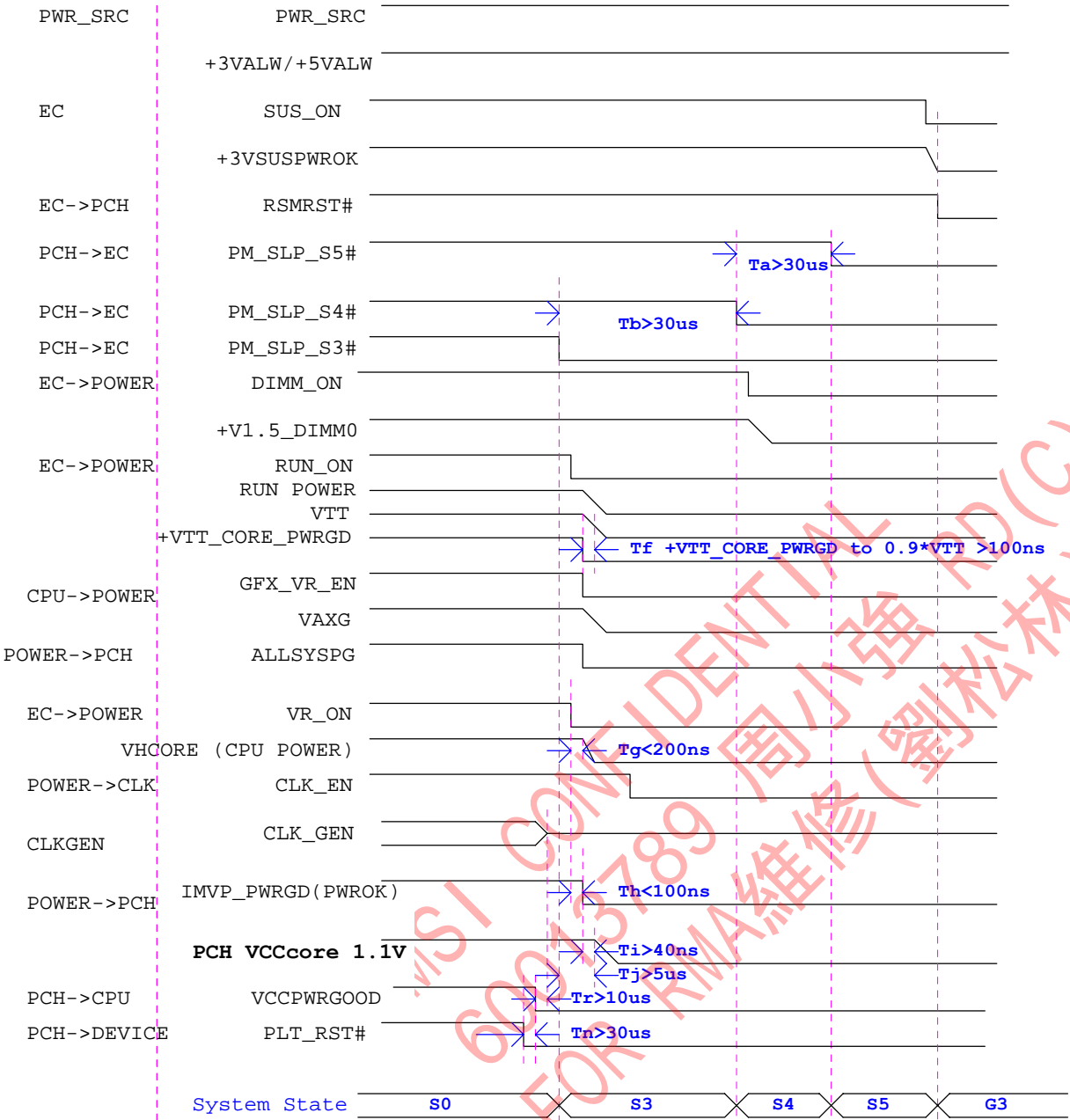
CONFIDENTIAL RD(C)201105160013789 周小強 (劉松林) ONLY

MSI MICRO-STAR INT'L CO.,LTD.	
Title	
EMI	
Size B	Document Number
MS-1681	
Date:	Thursday, December 17, 2009
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Rev	10

Calpella System Power on Sequence DC mode



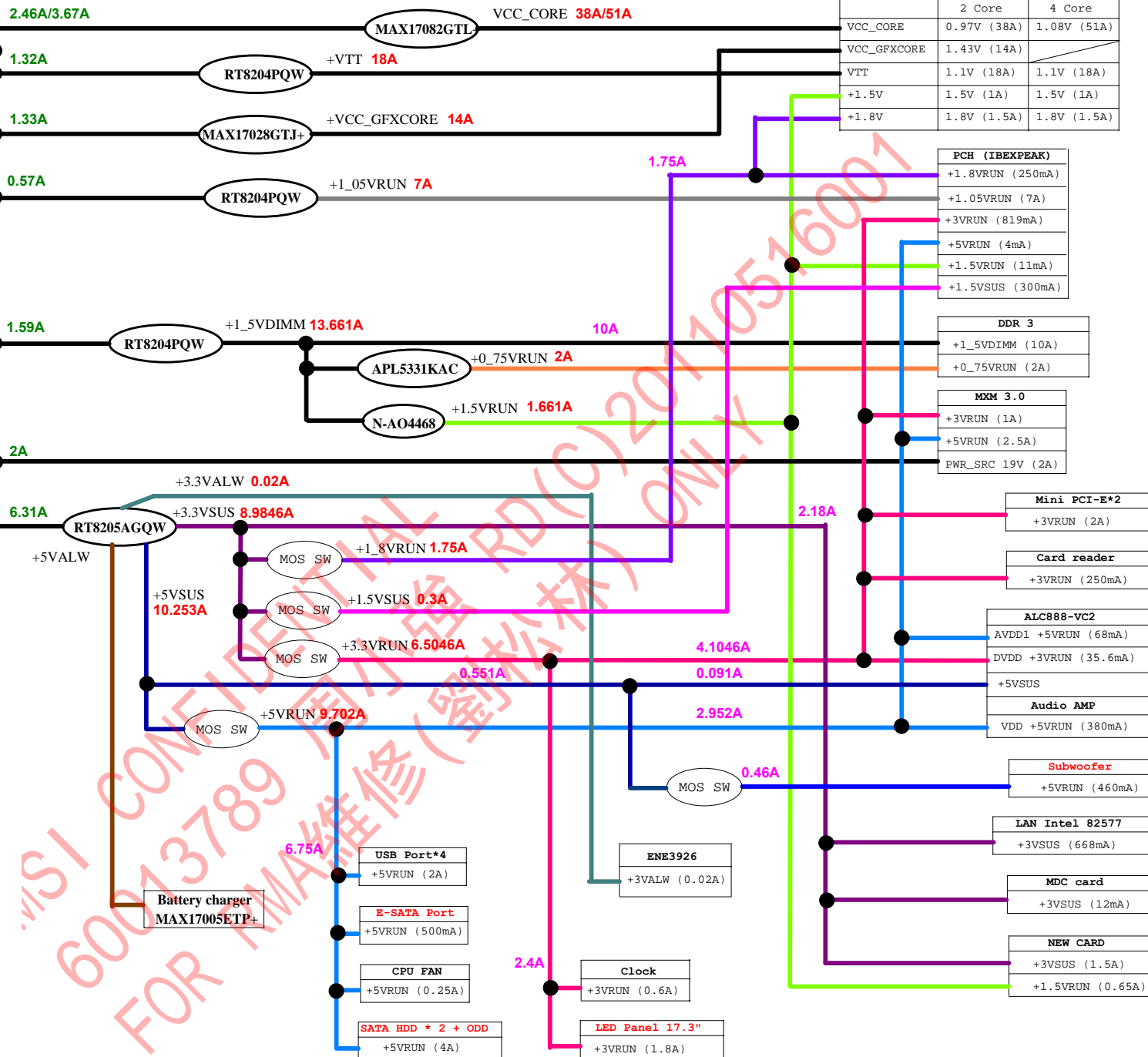
Power down Sequence DC mode S0 to G3



PWR_SRC

BAT : 3S2P = 9V
3S3P = 9V

VCC_CORE(2 Core) = 38A
VCC_CORE(4 Core) = 51A
+VTT(1.05V) = 18A
+VCC_GFXCORE = 14A
+1_05VRUN = 7A
+1_5VDIMM = 13.661A
+0_75VRUN = 2A
+1.5VRUN = 1.661A
+3.3VALW = 0.02A
+3.3VSUS = 8.9846A
+1_8VRUN = 1.75A
+1.5VSUS = 0.3A
+3.3VRUN = 6.5046A
+5VSUS = 10.253A
+5VRUN = 9.702A



CPU Auburndale/Clarksfield(989)		
	2 Core	4 Core
VCC_CORE	0.97V (38A)	1.08V (51A)
VCC_GFXCORE	1.43V (14A)	
VTT	1.1V (18A)	1.1V (18A)
+1.5V	1.5V (1A)	1.5V (1A)
+1.8V	1.8V (1.5A)	1.8V (1.5A)

2008/11/13 修改

Change Note :

0A-->0B

- 1.P19 stuff R113 & C85 for intel document about Braidwood
- 2.P23 add one PWM Pin for co-lay LED panel by EC
- 3.P25 Change CardReader to ENE
- 4.P26 Change "LED_HDD#" PU +5VRUN to +3VRUN
- 5.P26 Fan conn footprint change back to "53398_03"
- 6.P28 Add Wireless & Bluetooth combo(MS-3870)
- 7.P32 Change PR171 to 48.7K & PR172 to 1R0603
- 8.P33 Change PU2 from "UP6182AQAG" to "TPS51125" & PR18 to 30K
- 9.P34 Change PU9 from "UP6111AQDD" to "UP6128A" & PR156 to 3.48K & PR159 to 10.7K & PQ10 to "D03-0443033-V02"
- 10.P35 Change PU8 from "UP6111AQDD" to "UP6128A" & PR149 to 4.22K & remove C394
- 11.P36 Change PR95 to 1.82K & PR29 to 9.31K & PC90 to 47nf & PR99 to 931R & no stuff PC84 , PR94 , PEC4 , PEC5 , PEC6 , PEC8

0B-->10

- 1.P13 add net "TP_HDA_DOCK_EN#_R" for flash protect control.
- 2.P14 add wimax ac adepter schematic.
- 3.P23 add ENE GPIO13 for flash protect control.
- 4.P25 no stuff C399 & C400 for cardreader detect issu.
- 5.P26 change R307 from 0R to 33R for EMI.
- 6.P31 add 2 cap in +VBATA for EMI.
- 7.P34 change R329 from 0R to 1K for current limit.
- 8.P37 no stuff +VCC_GFXCOPE PQ23 no cost down.
- 9.P40 change JNCB2 to RB3 , and 33R for EMI.
- 10.P40 change CB2 from 0.1u to 300p for EMI.
- 11.P13 No stuff for MP ver PCH by R289 , R271 , R298 , R291 , R297 , R290.

10-->11

- 1.P37 add "PC1" & modify "PR12" & "PC104" for power shut down issue.